

Compal Confidential

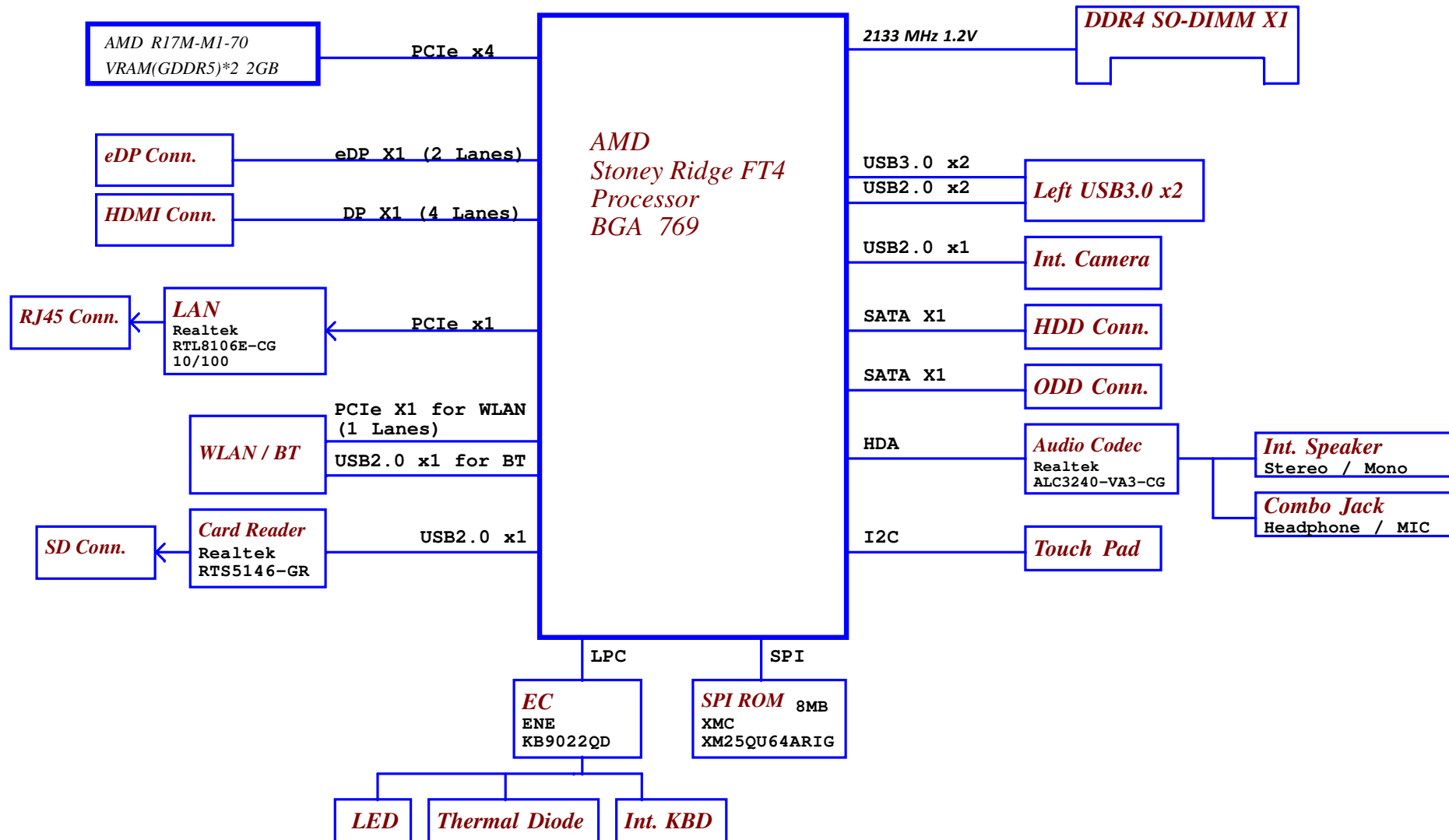
DIS M/B Schematics Document

AMD Stoney Ridge FT4

LA-G241P
2018-03-12
REV : 1 . 0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2018/03/12	Deciphered Date	2019/03/12	
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AMD Stoney Ridge FT4



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Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.95VALW	0.95V always on power rail	ON	ON	ON
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+1.2V	1.2V power rail for APU and DDR	ON	ON	OFF
+2.5V	2.5V switched power rail for DDR	ON	ON	OFF
+0.6V	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVBATT	RTC power	ON	ON	ON
+0.775VALW	0.775V always on power rail	ON	ON	ON

	SOURCE	APU	BATT	NPCE388N	SO-DIMM	WLAN	Thermal Sensor
EC_SMB_CK1 EC_SMB_DA1	ENE9022 +3VL	X	V +3VALW	X	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	X	X
EC_SMB_CK2 EC_SMB_DA2	ENE9022 +3VS	V +1.8VS	X	X	X	X	V +3VS

Device	Address
Smart Battery	0001 011x b
Charger	0001 0010 b

Device	Address	HEX
APU	1001 100X b	98H

Device	Address
DDR DIMM1	1010 000X b

Device	Address	HEX
GPU	0100 0001 b	0X41H

Port	Device
0	LAN
1	
2	WLAN
3	

USB 3.0	USB 2.0	3 External USB Port
	0	
	1	WLAN/BT Combo
	2	Camera
	3	Card Reader
	4	
1	5	Left USB3.0 port 1
2	6	Left USB3.0 port 2
	7	

OC#	USB Port	
0		
1	USB2 port5	USB3 port1
2		
3		

UIC1 A9_9425@
A9_9425 R3
SA0000BGS20



ZZZ ODD@

PCB DLADE LA-G241P LS-G201P/G202P 02
DAZ29700101

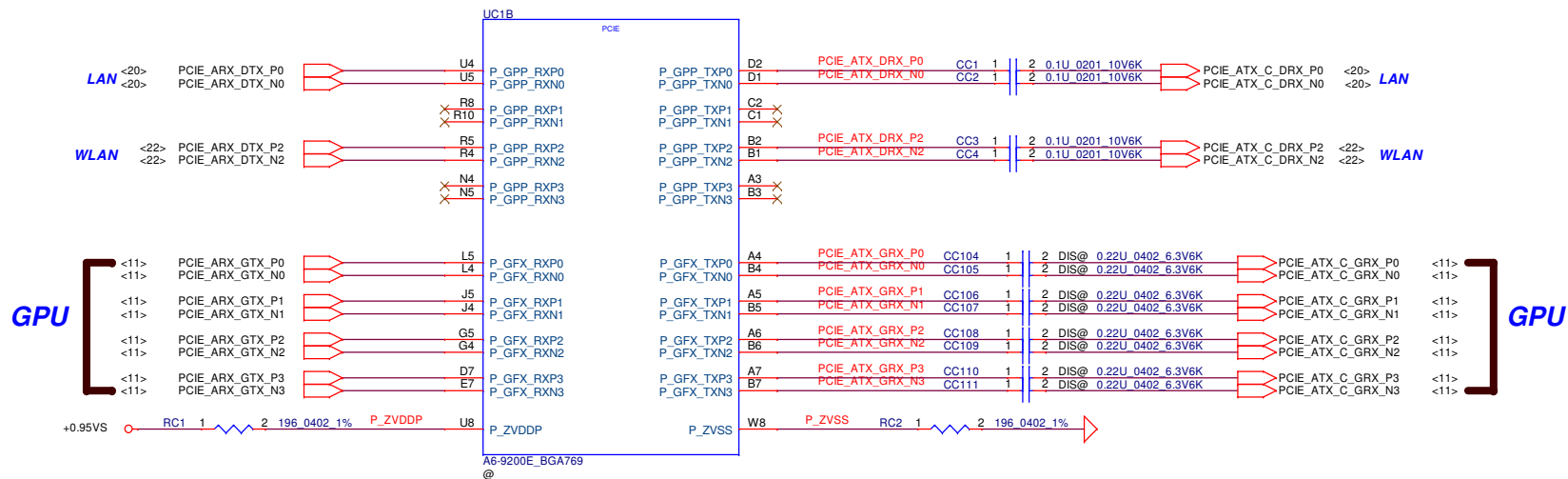


PCB DLADE LA-G241P LS-G201P 02
DAZ29700201

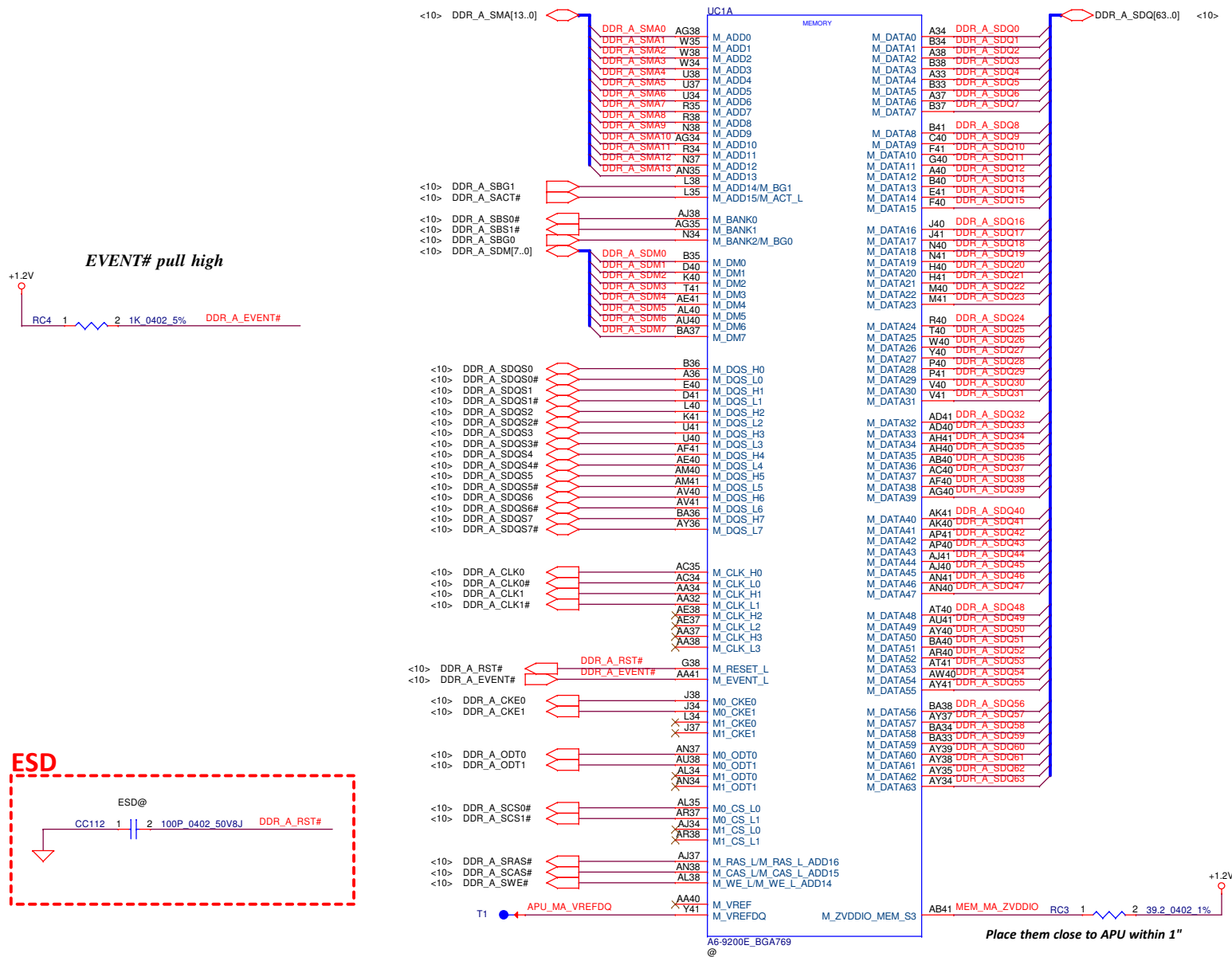
<i>STATE \ SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>Full ON</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S1 (Power On Suspend)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>LOW</i>
<i>S3 (Suspend to RAM)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

[illegible]

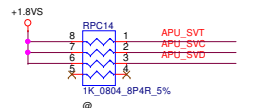
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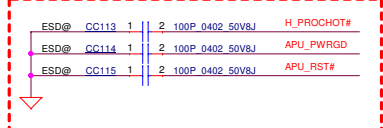
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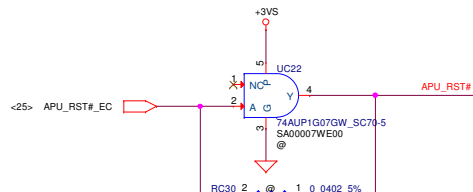
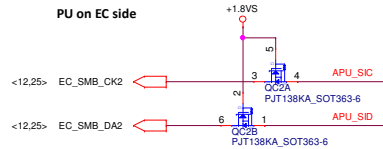
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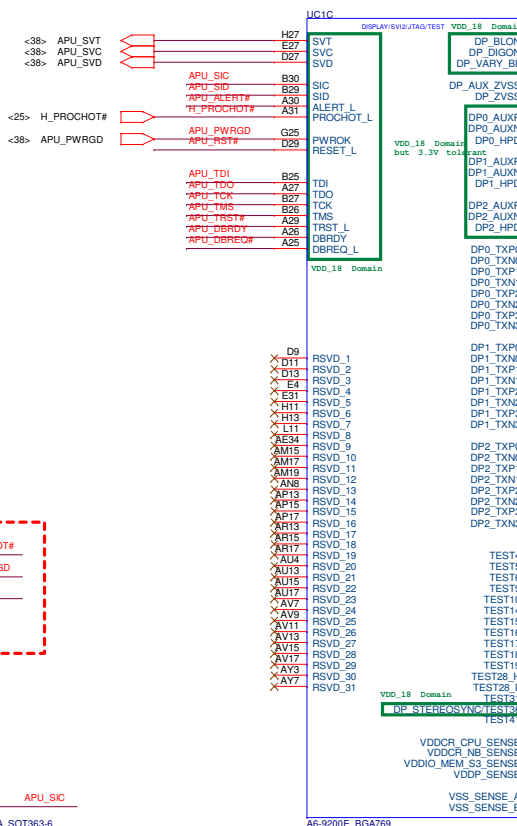
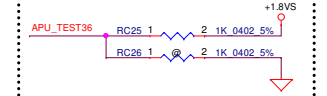
ESD



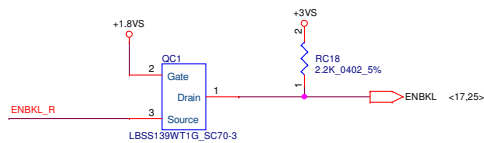
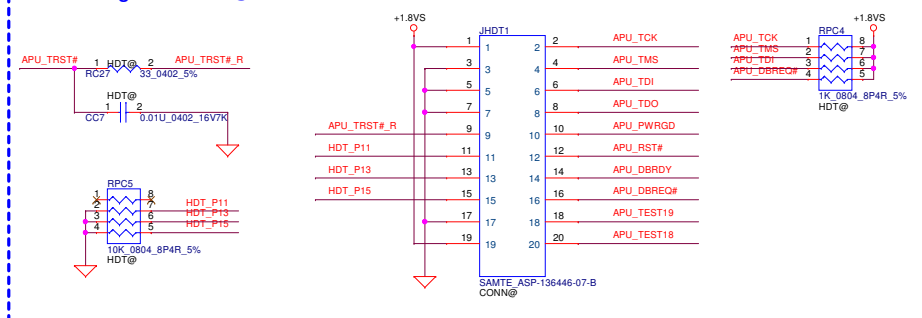
PU on EC side



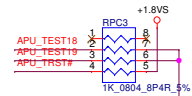
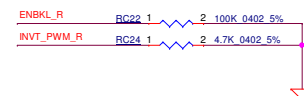
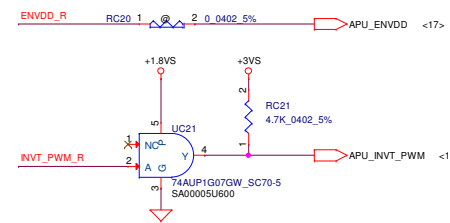
Stoney Ridge FP4_FT4 Interlock July_2017 ver 2.1:
To enable HDMI, it must be pulled up to 1.8V_50 rail
by 1K ohm resistor



HDT+ Debug conn - HDT@



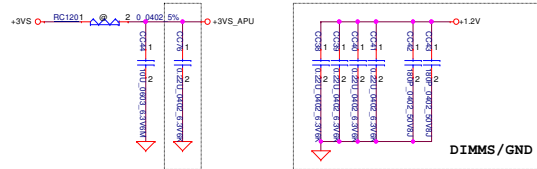
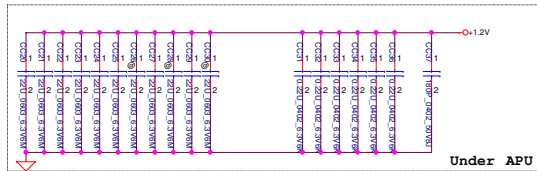
+LCDVDD_CONN PWR switch enable pin VIH=1.2V



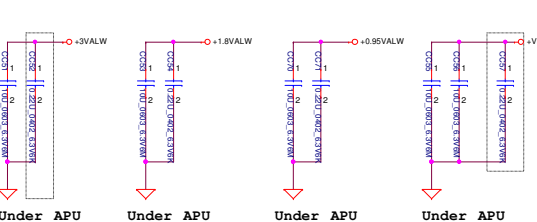
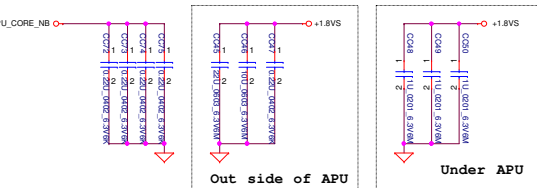
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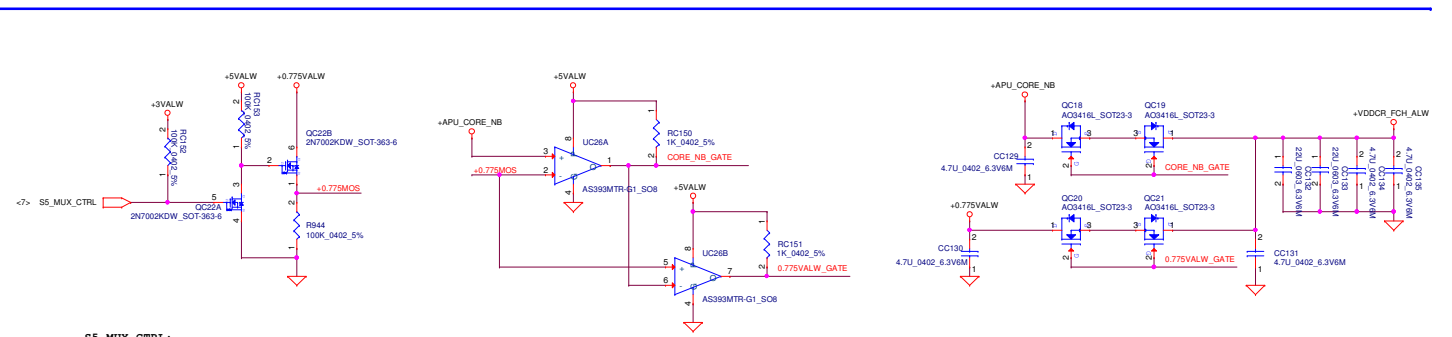
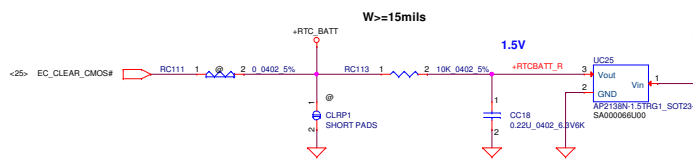
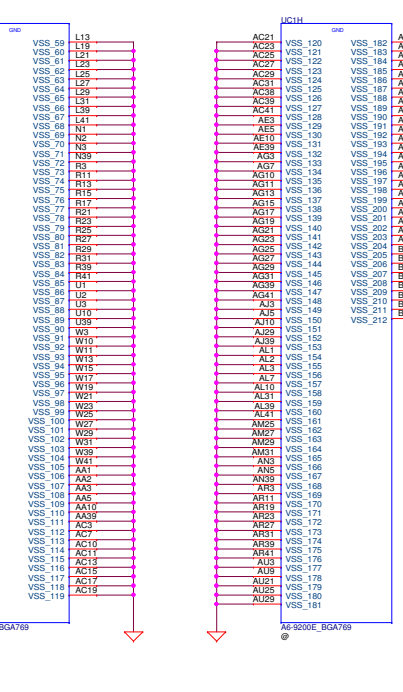
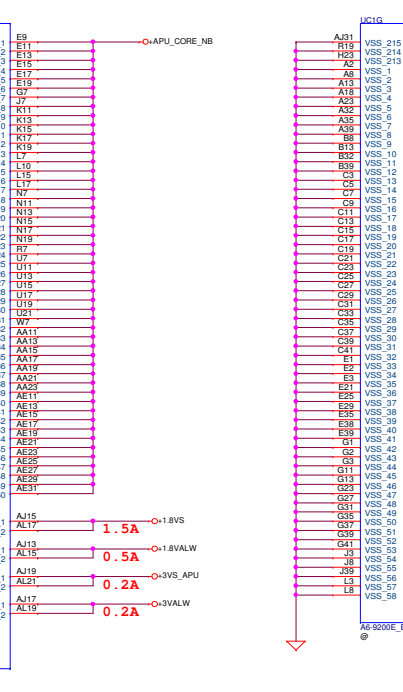
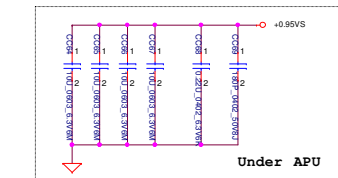
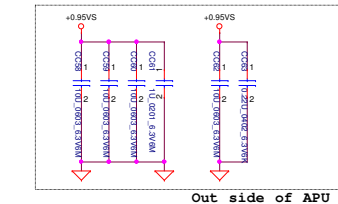
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Under APU ACROSS +1.2V_VDDQ AND VSS SPLITT

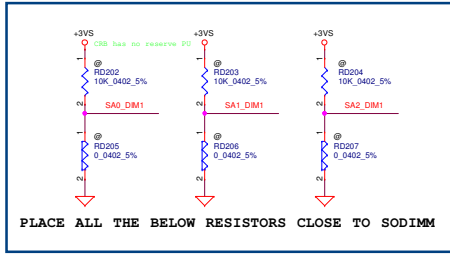


+0.95VS OF APU



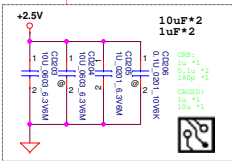
SS_MUX_CTRL:
Enable MUX (S0 to S3)--->LOW
Disable MUX (S3 to S0)--->HIGH

Stoney So-DIMM1

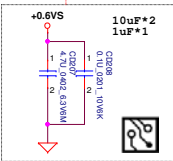


SPD ADDRESS FOR CHANNEL A :
SA0 = 0; SA1 = 0; SA2 = 0.

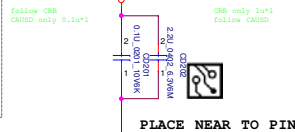
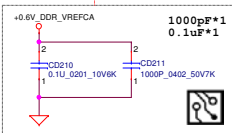
Layout Note:
Place near JDIMM1.257,259



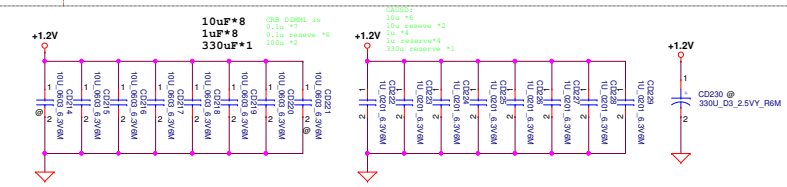
Layout Note:
Place near JDIMM1.258



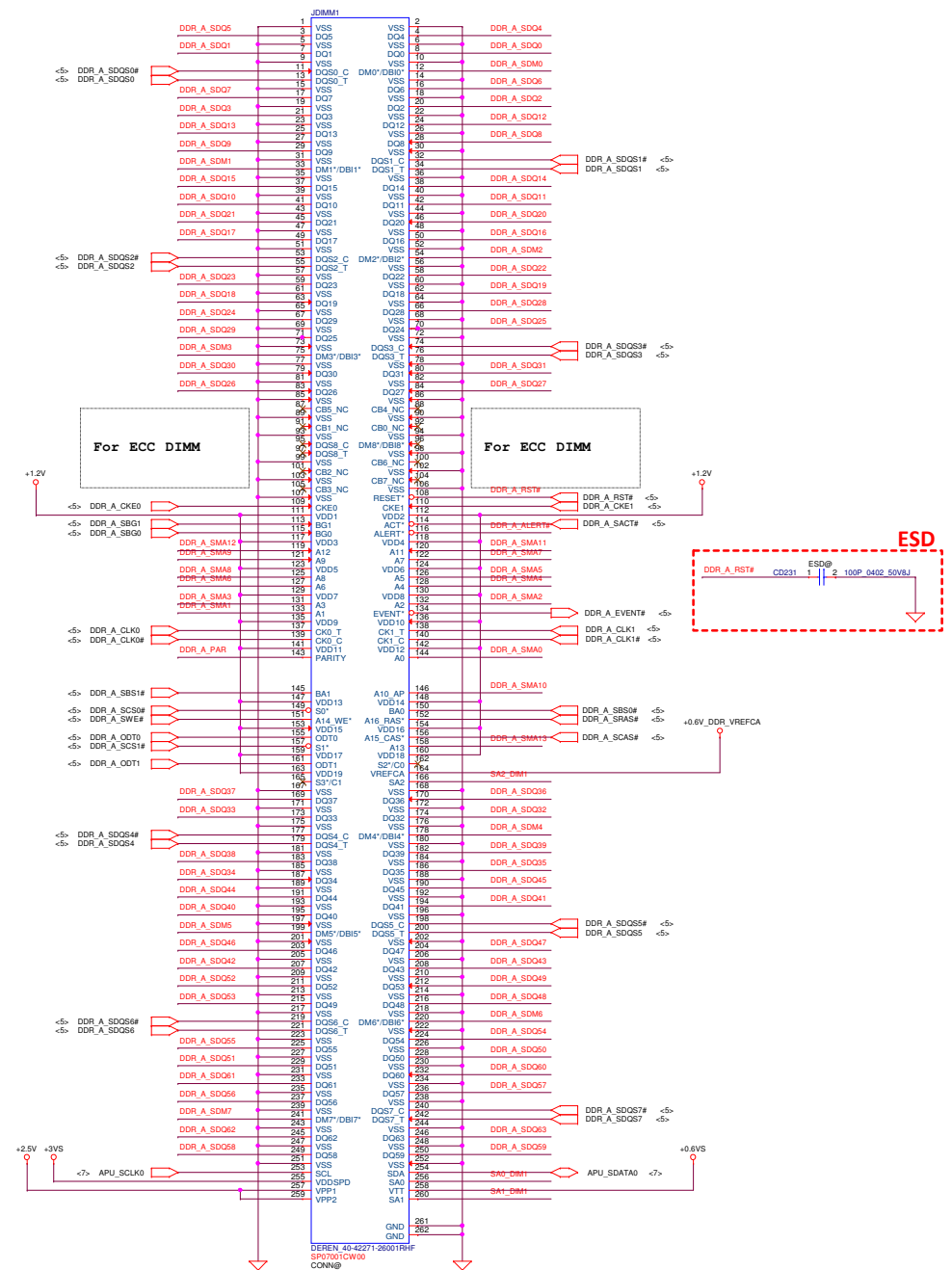
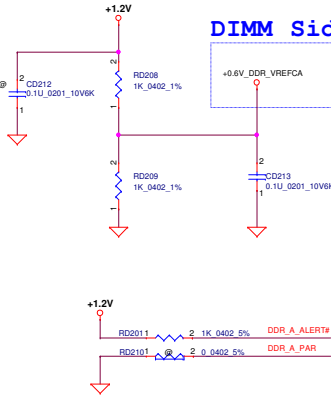
Layout Note:
PLACE THE CAP near JDIMM1. 164



Layout Note:
Place near JDIMM1



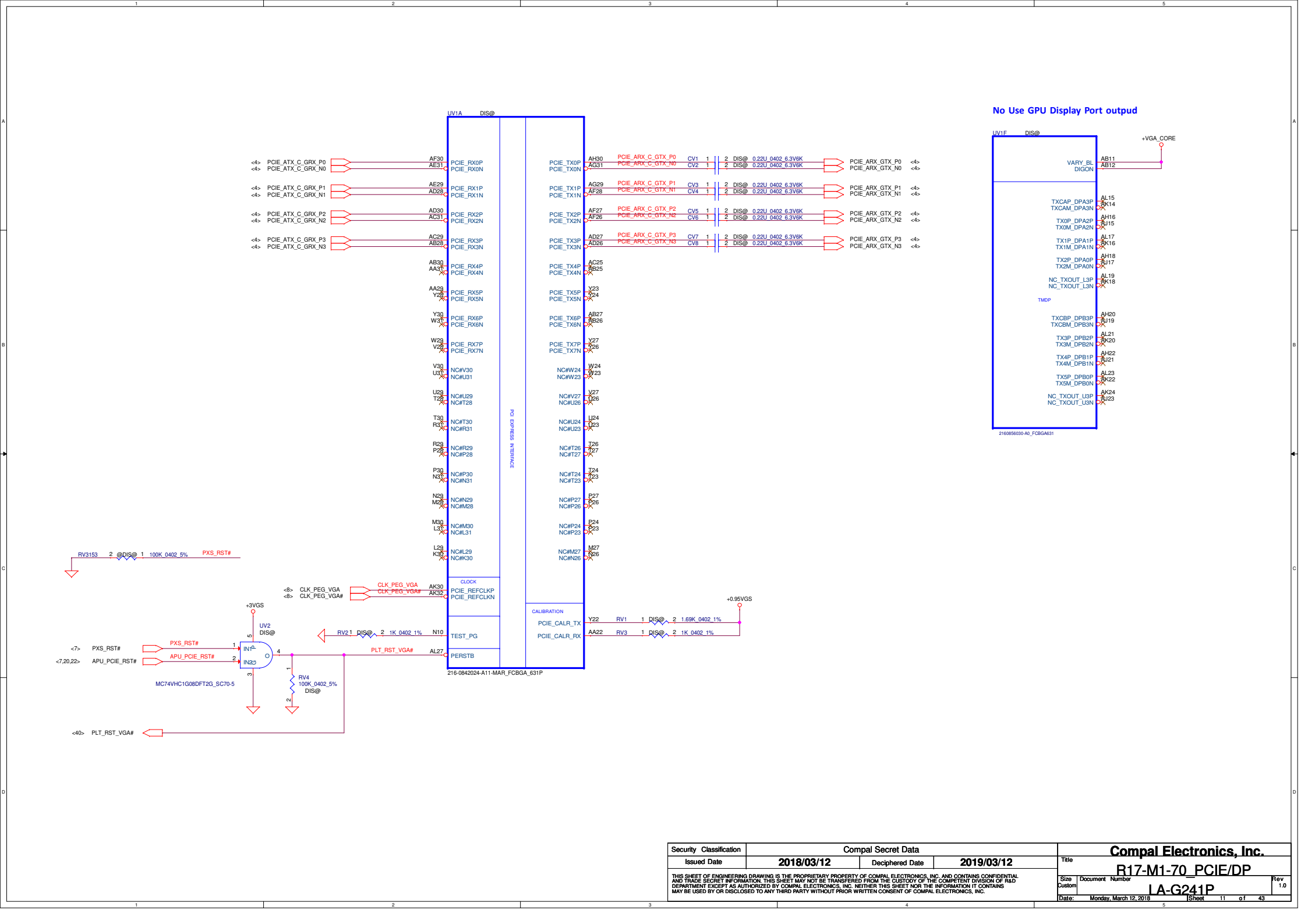
DIMM Side

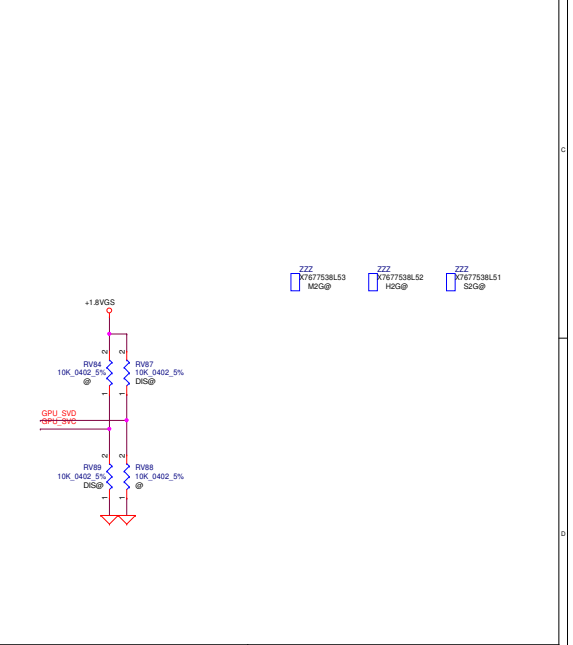
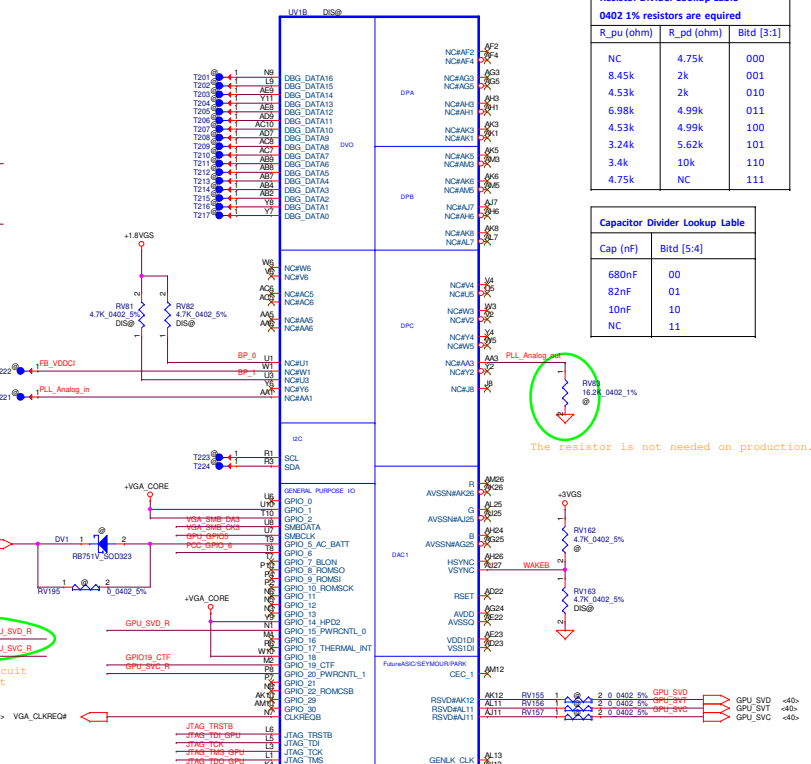


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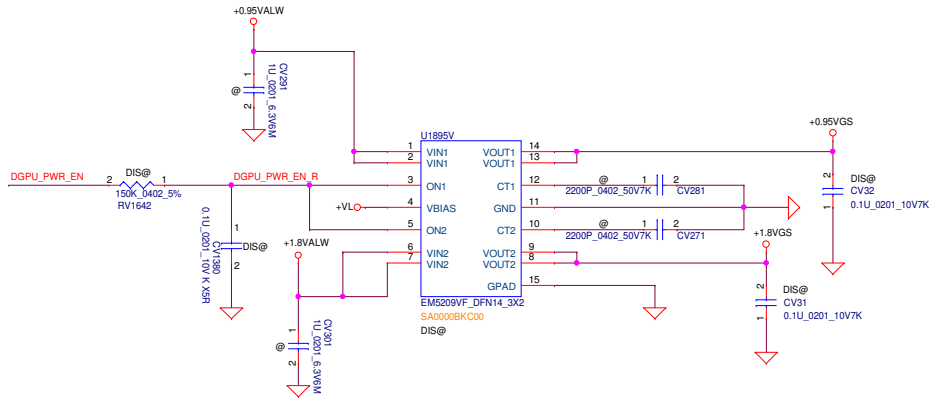




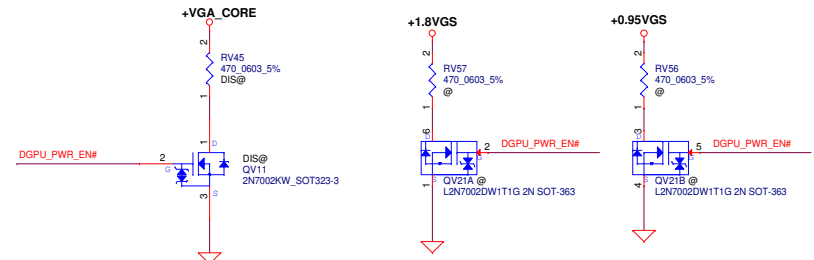
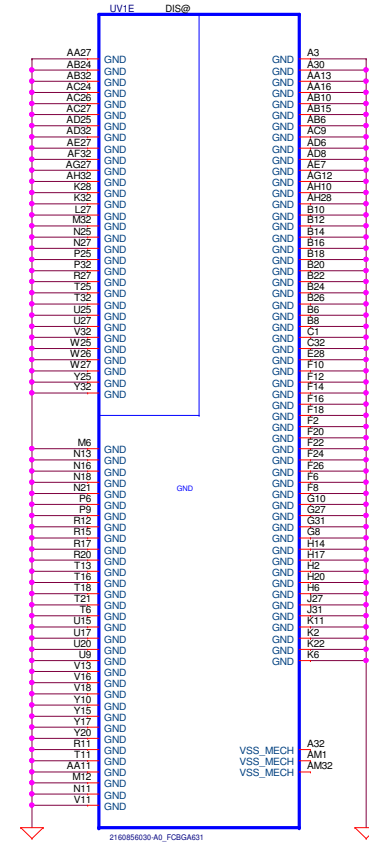
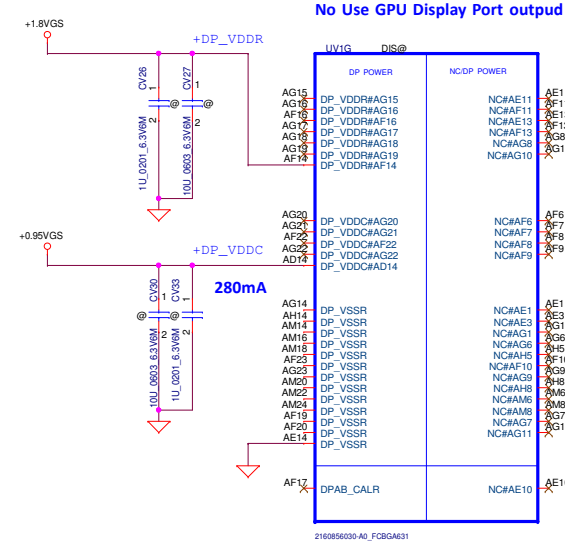
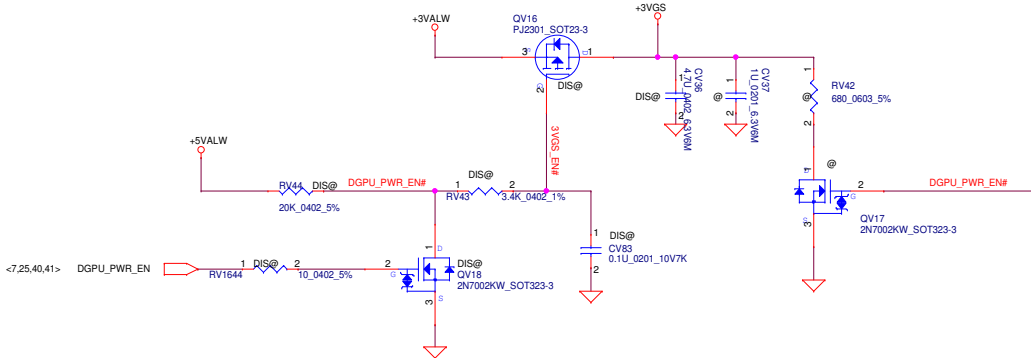
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

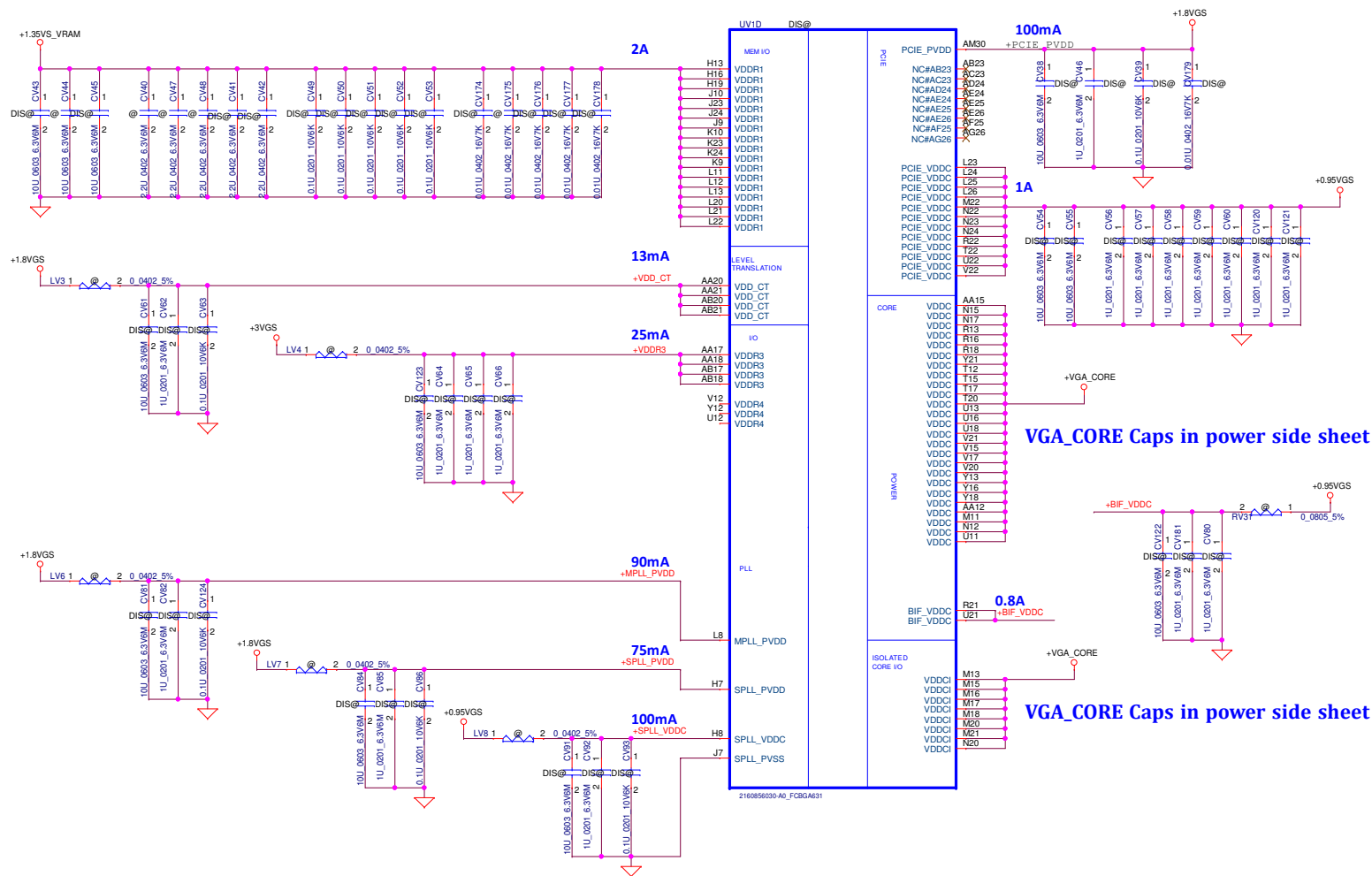
**+1.8VALW TO +1.8VGS
+0.95VALW TO +0.95VGS
Load switch**



+3VALW to +3VGS



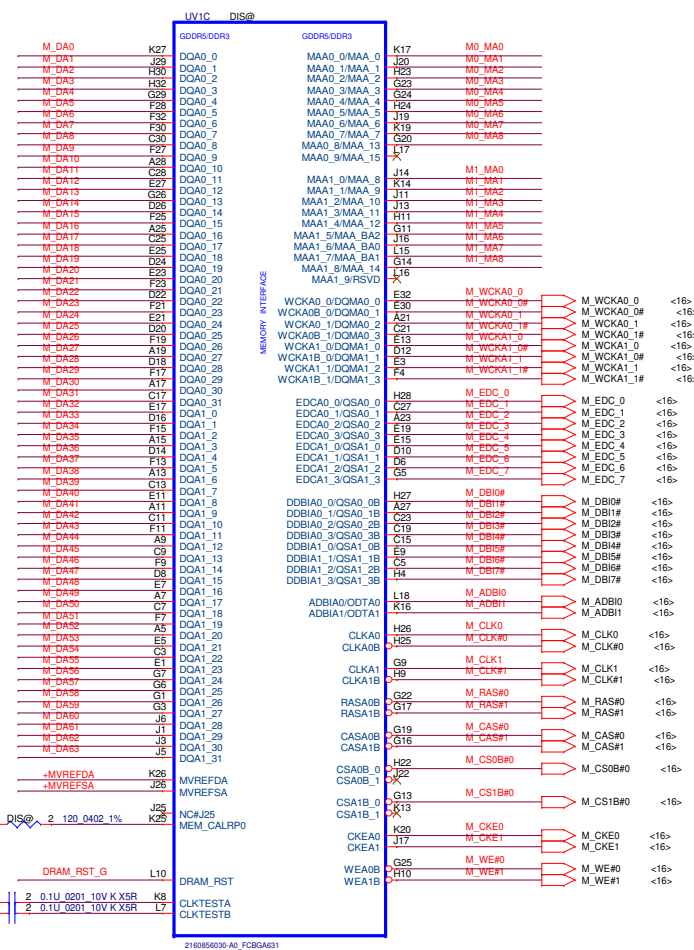
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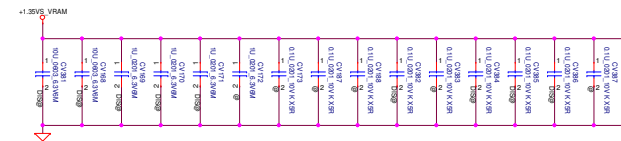
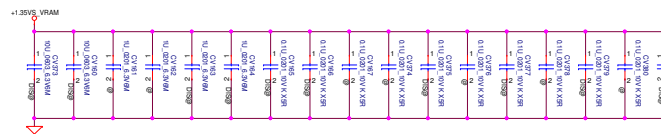
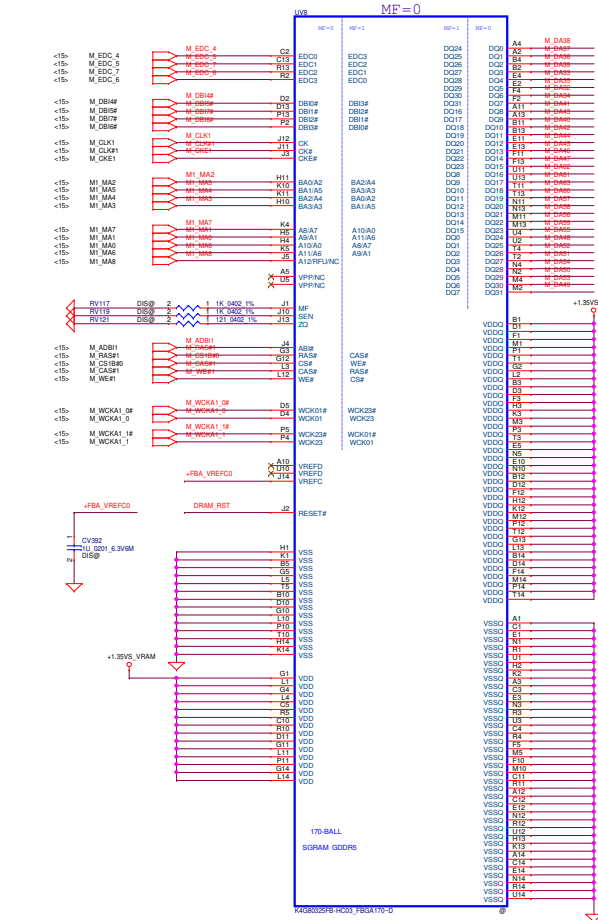
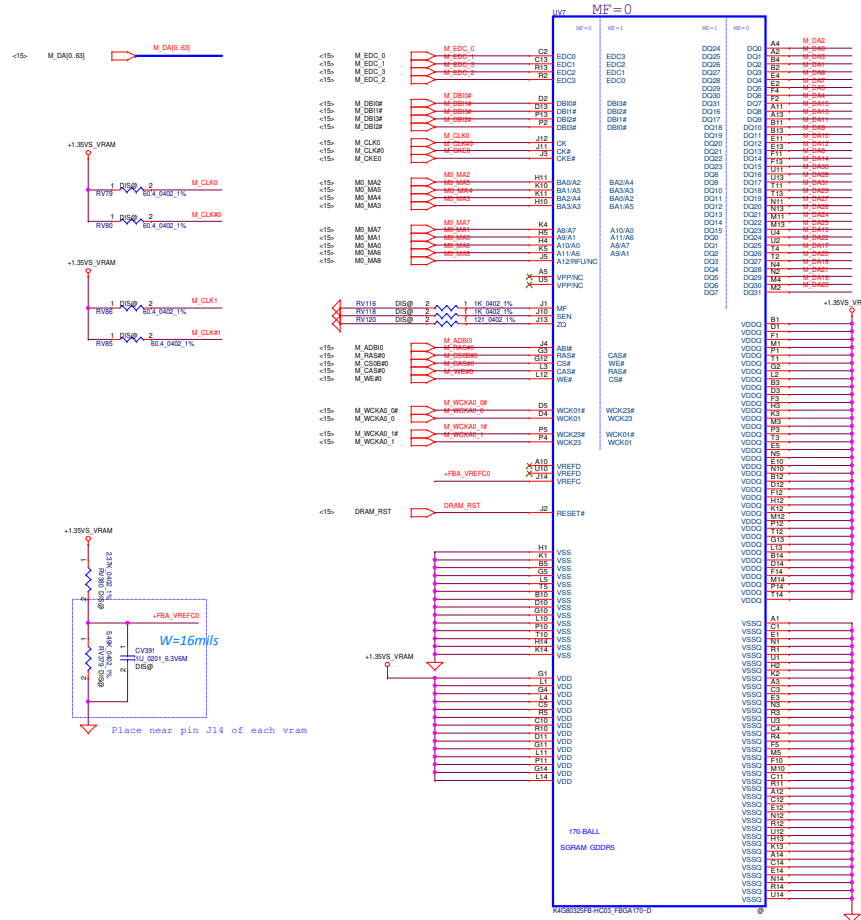
VGA_CORE Caps in power side sheet

VGA_CORE Caps in power side sheet

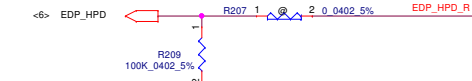
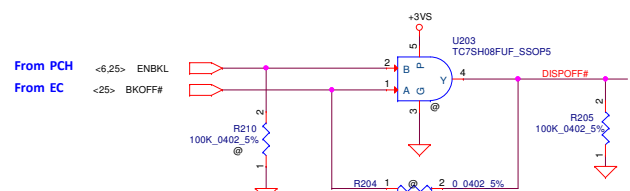
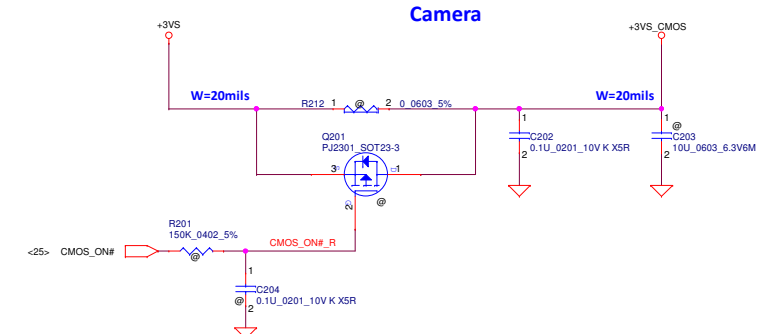
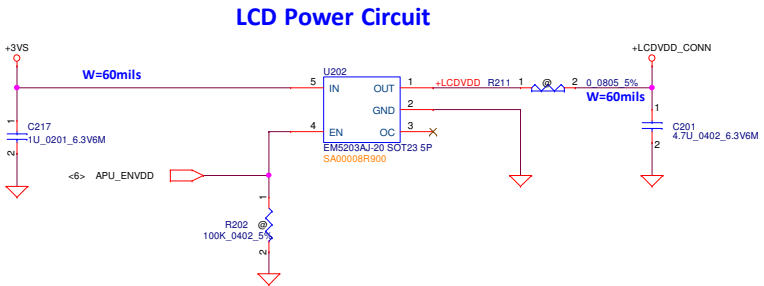
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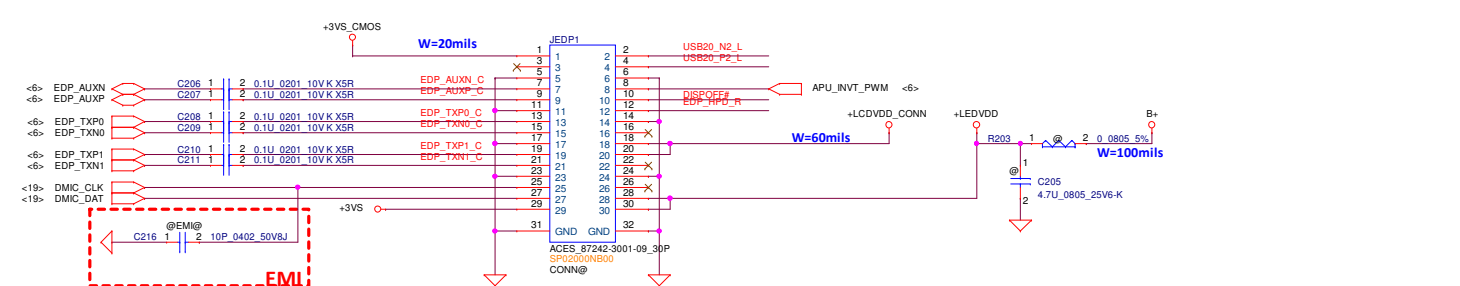
Memory Partition A



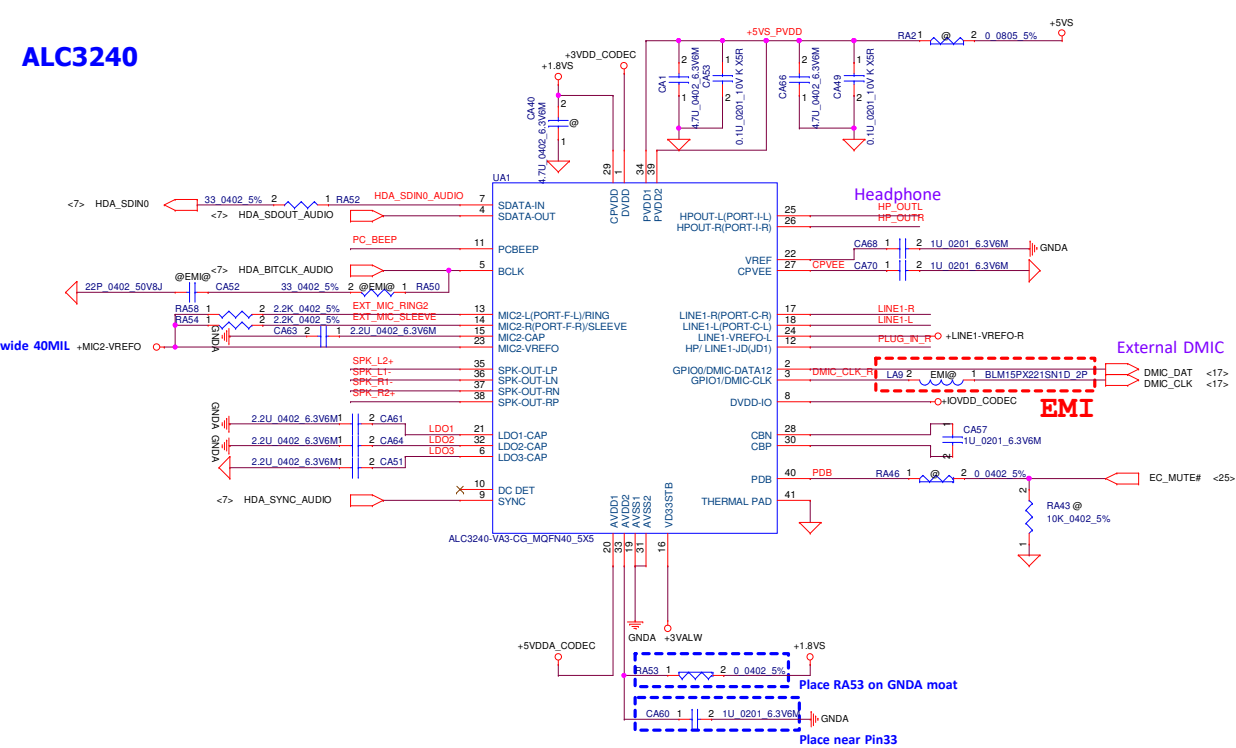
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Issued Date	2016/03/12	Deciphered Date	2019/03/12	GDDR5	
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LA-G241P				Date	Monday, March 12, 2018



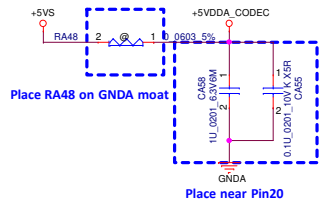
eDP CONN.



ALC3240



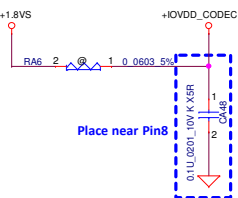
+5VS to +5VDDA_CODEC



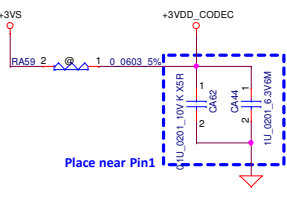
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	3.3V	1.8V	1.5V
AMD Carrizo-L			V
AMD Stoney Radege FT4		V	

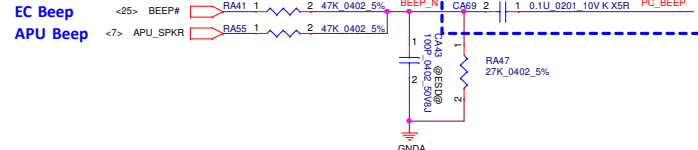
+1.8VS to +IOVDD_CODEC (For AMD FT4)



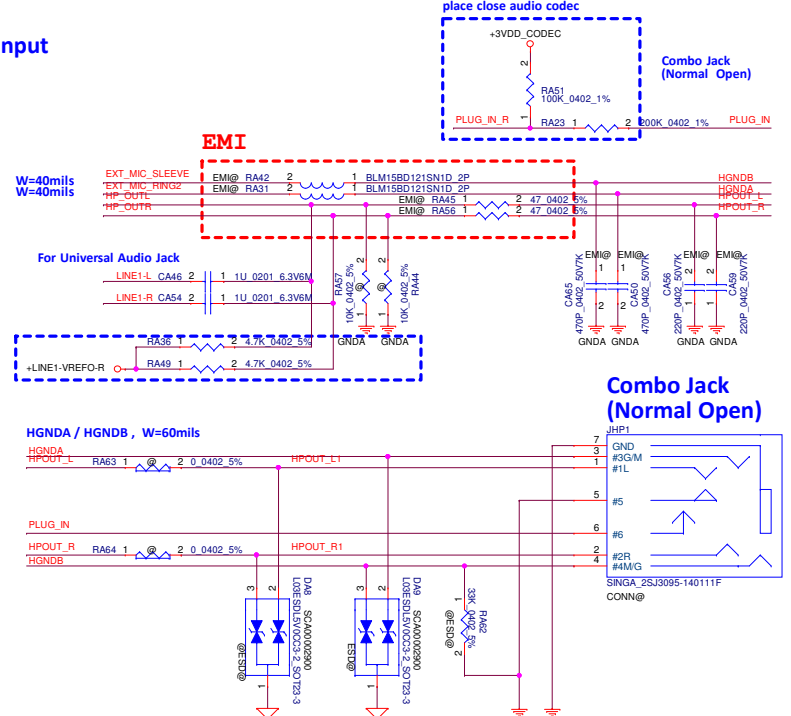
+3VS to +3VDD_CODEC



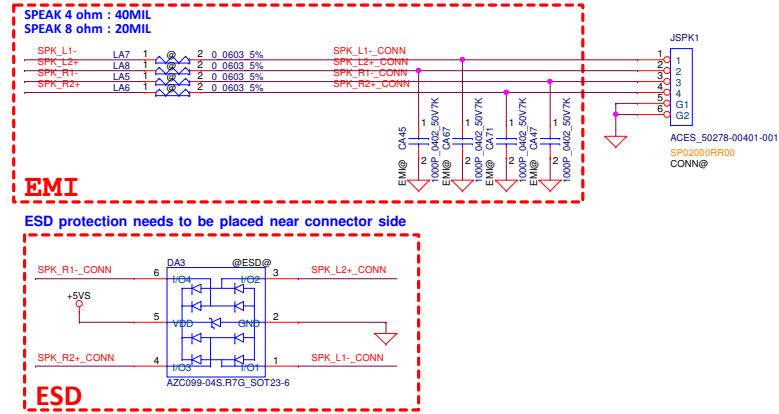
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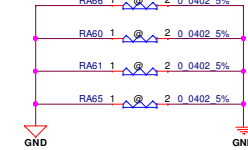
Input



Output

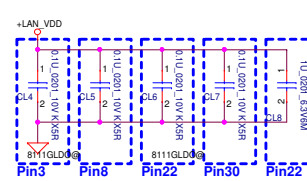
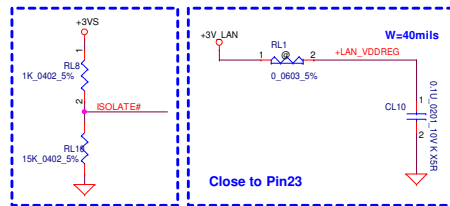
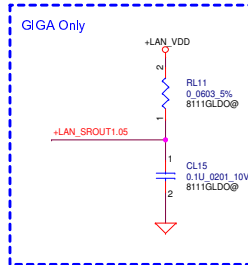
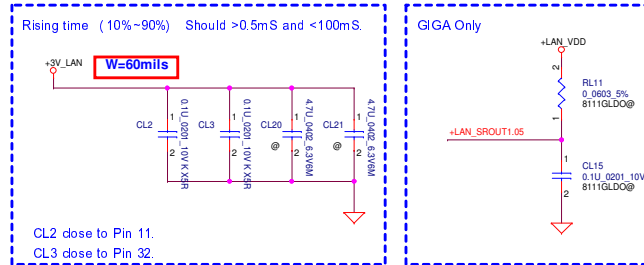
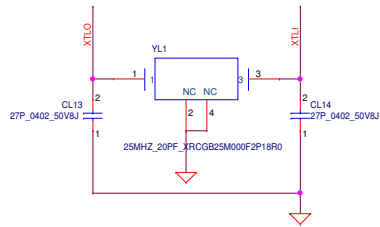
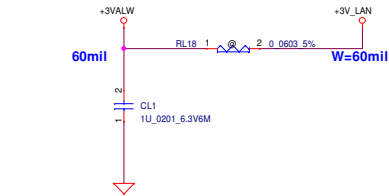


EMI

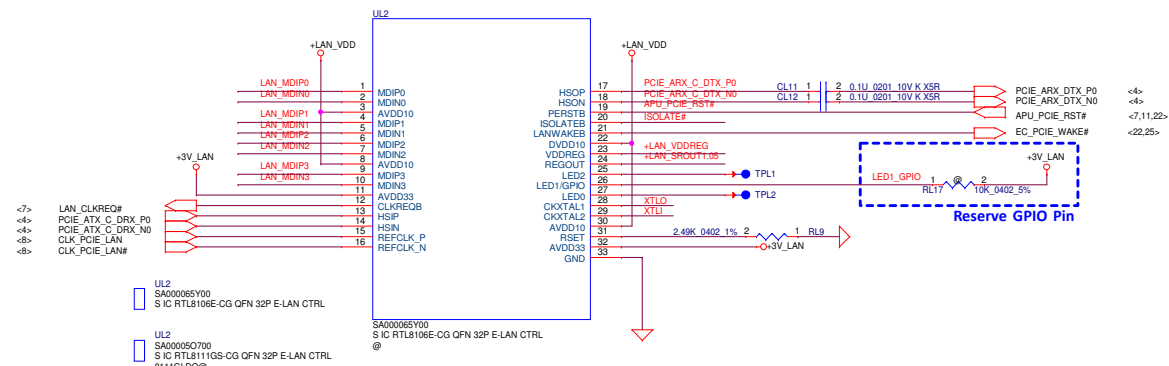
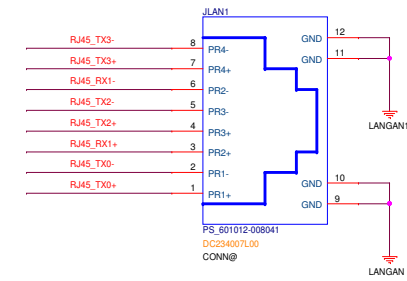


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Date: Monday, March 12, 2018				Rev 1.0
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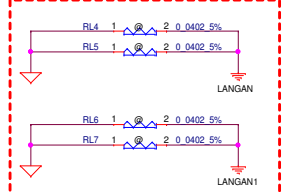
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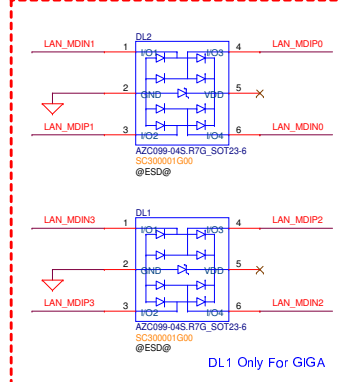
RJ-45 Connector



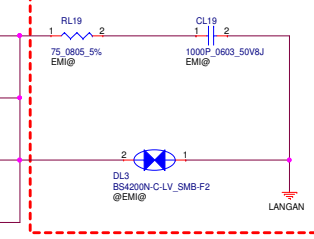
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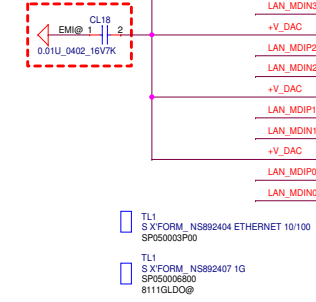
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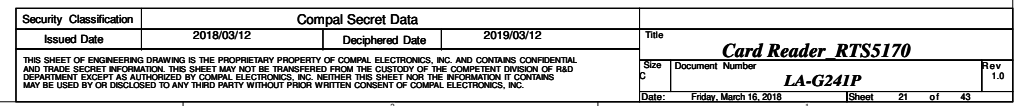
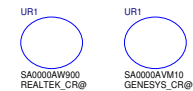
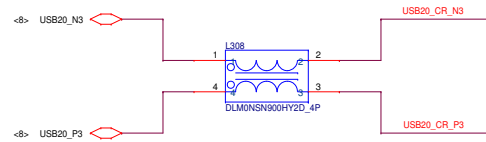
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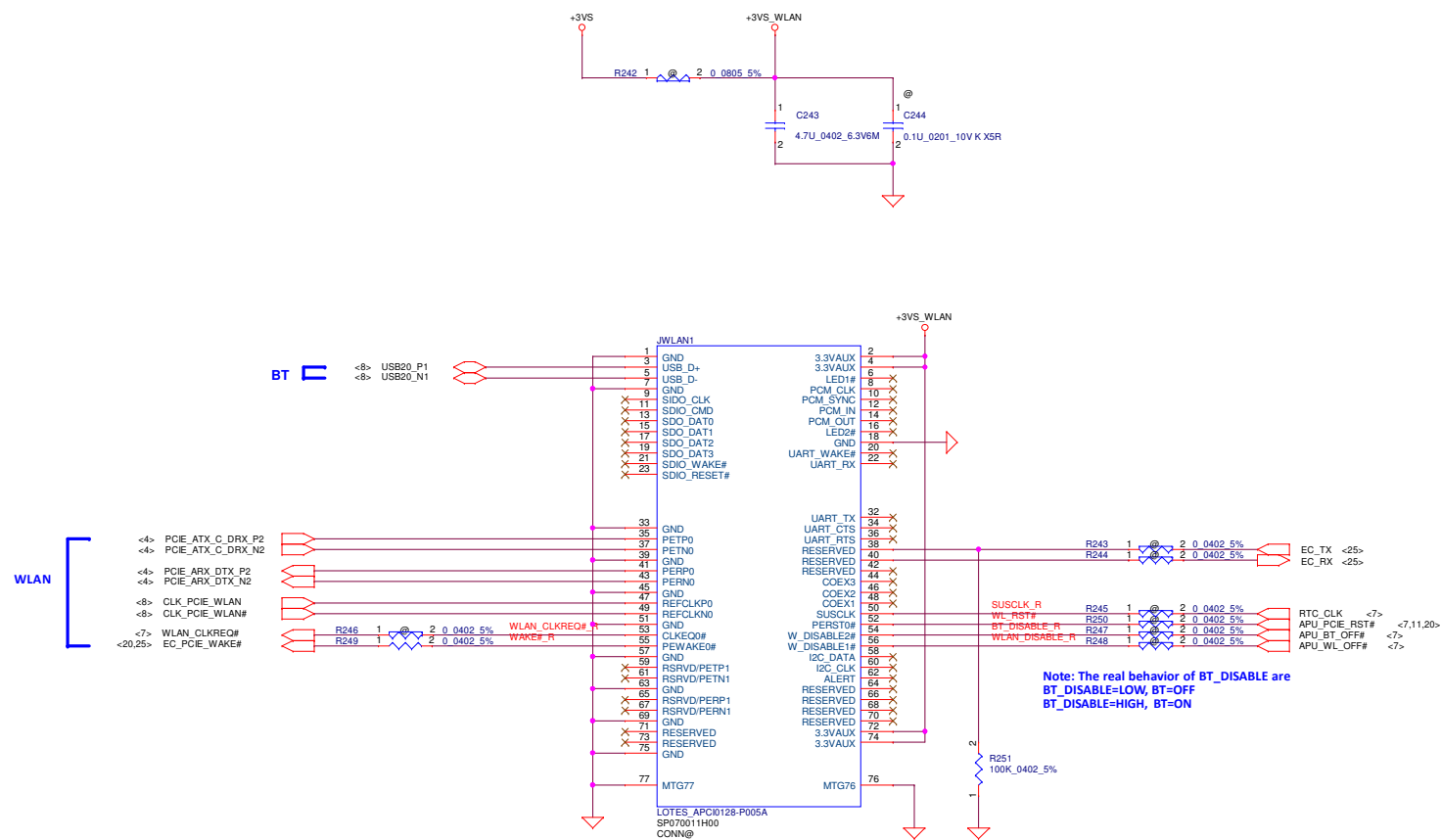
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Size	Document Number	Rev
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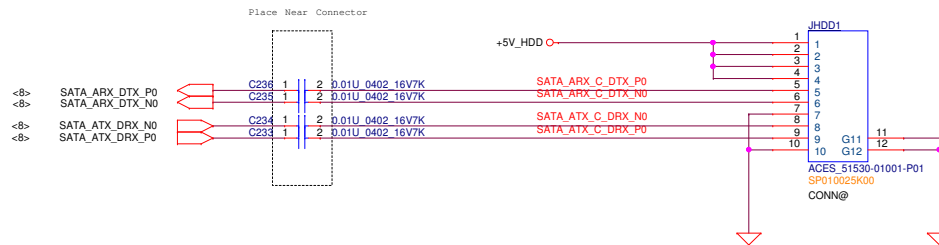
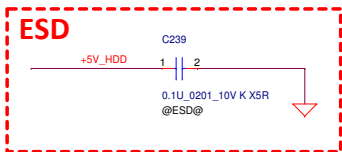
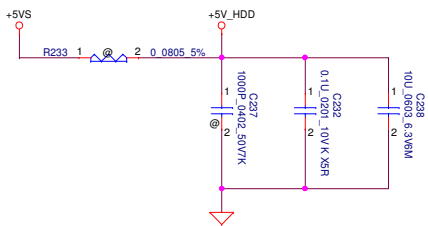


NGFF - WLAN / BT (E- KEY)



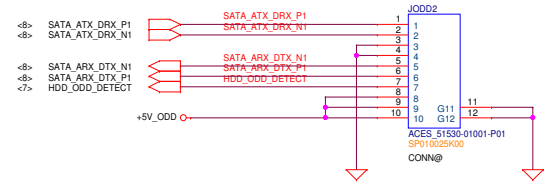
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				Size	Document Number
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HDD FFC Connector to Sub Board

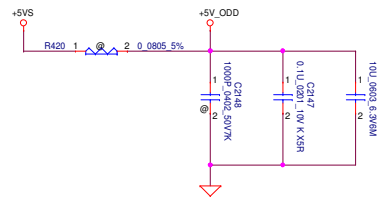


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ODD FFC Connector to Sub Board (15" Only)

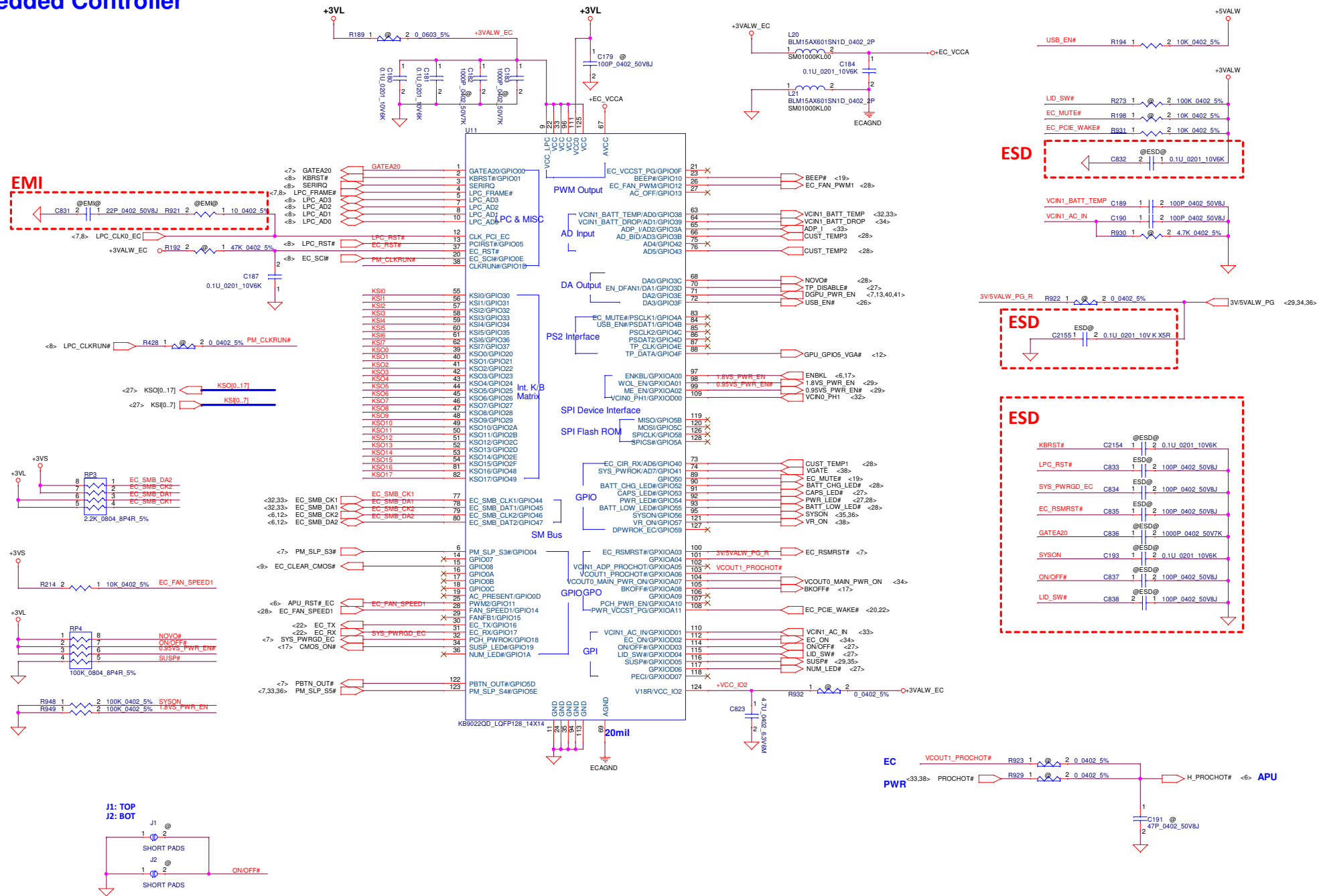


ODD MISC.



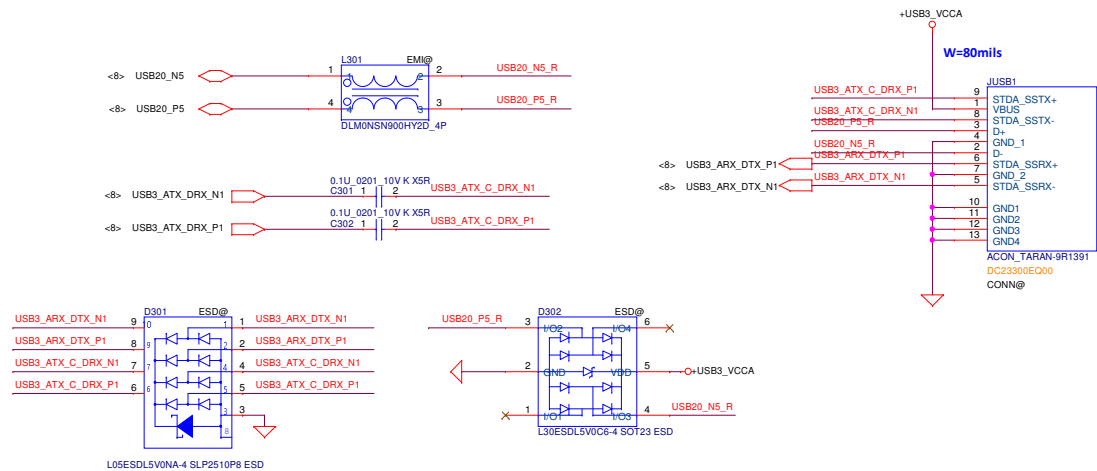
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Embedded Controller

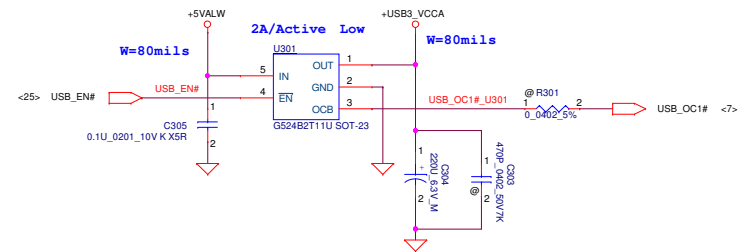
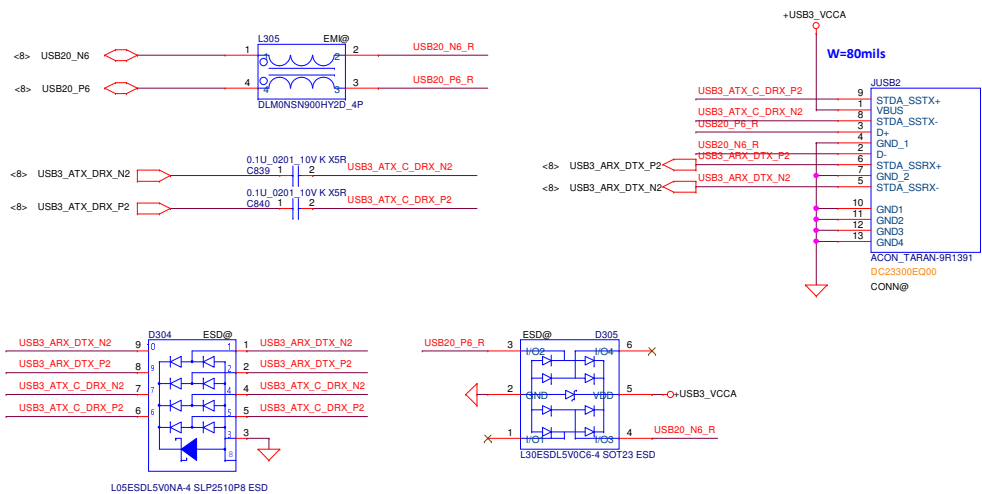


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USB 3.0 (PORT 1)

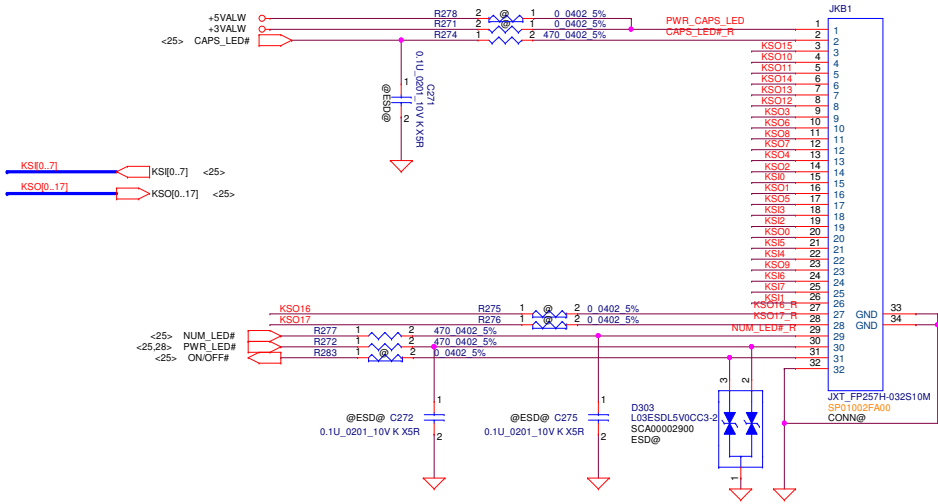


USB 3.0 (PORT 2)

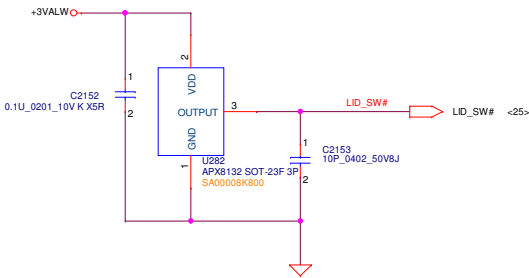


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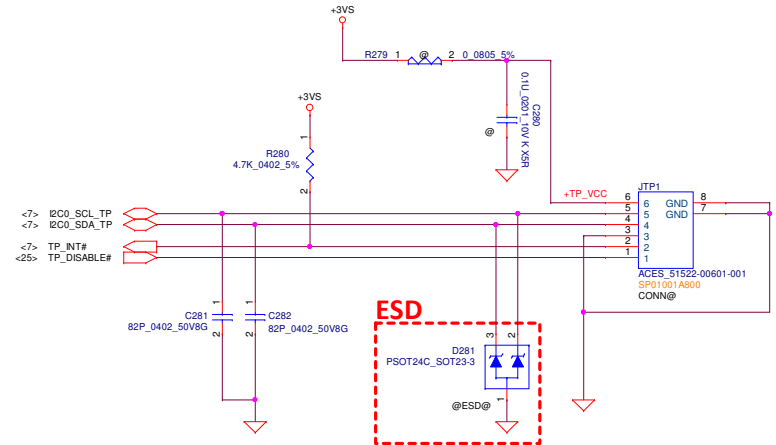
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Hall Sensor



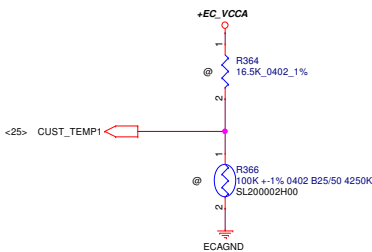
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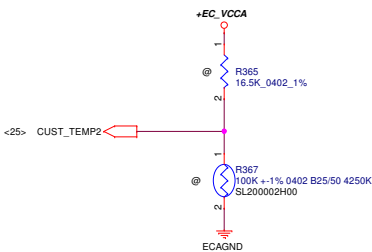
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Thermal Diode

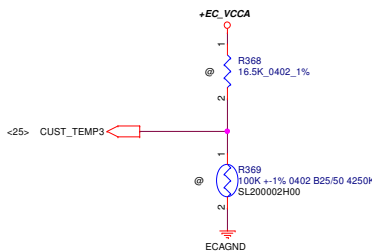
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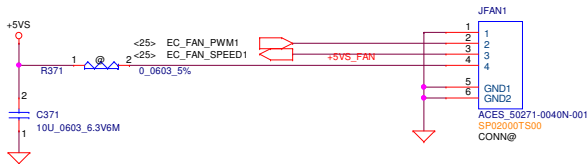
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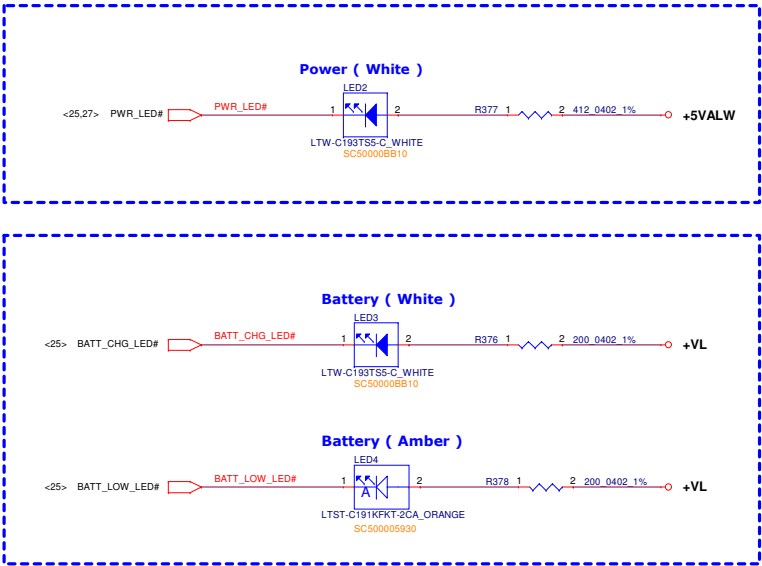
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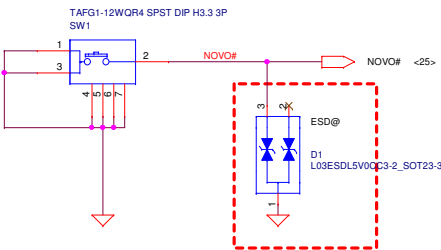
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LED

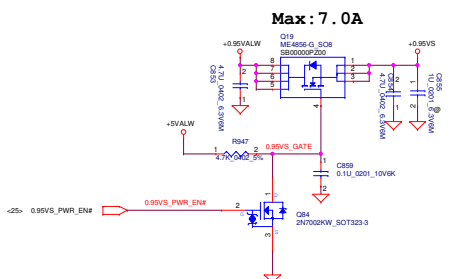
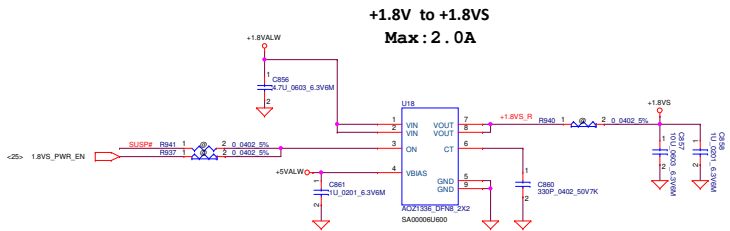
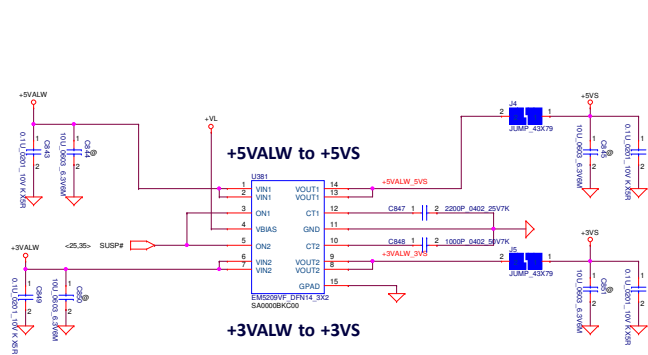


NOVO BUTTON

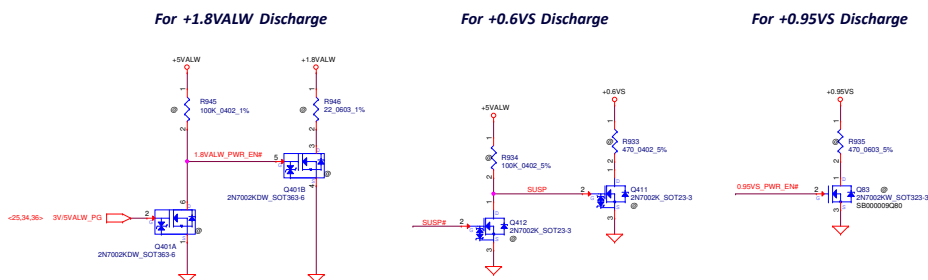


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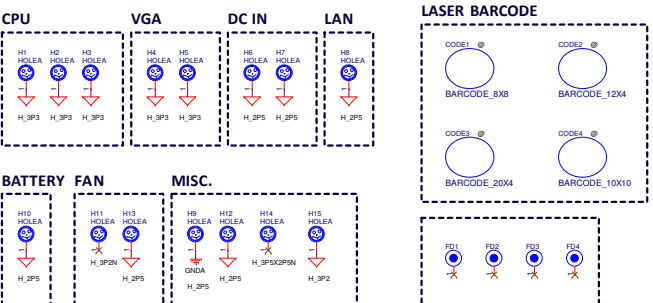
DC to DC



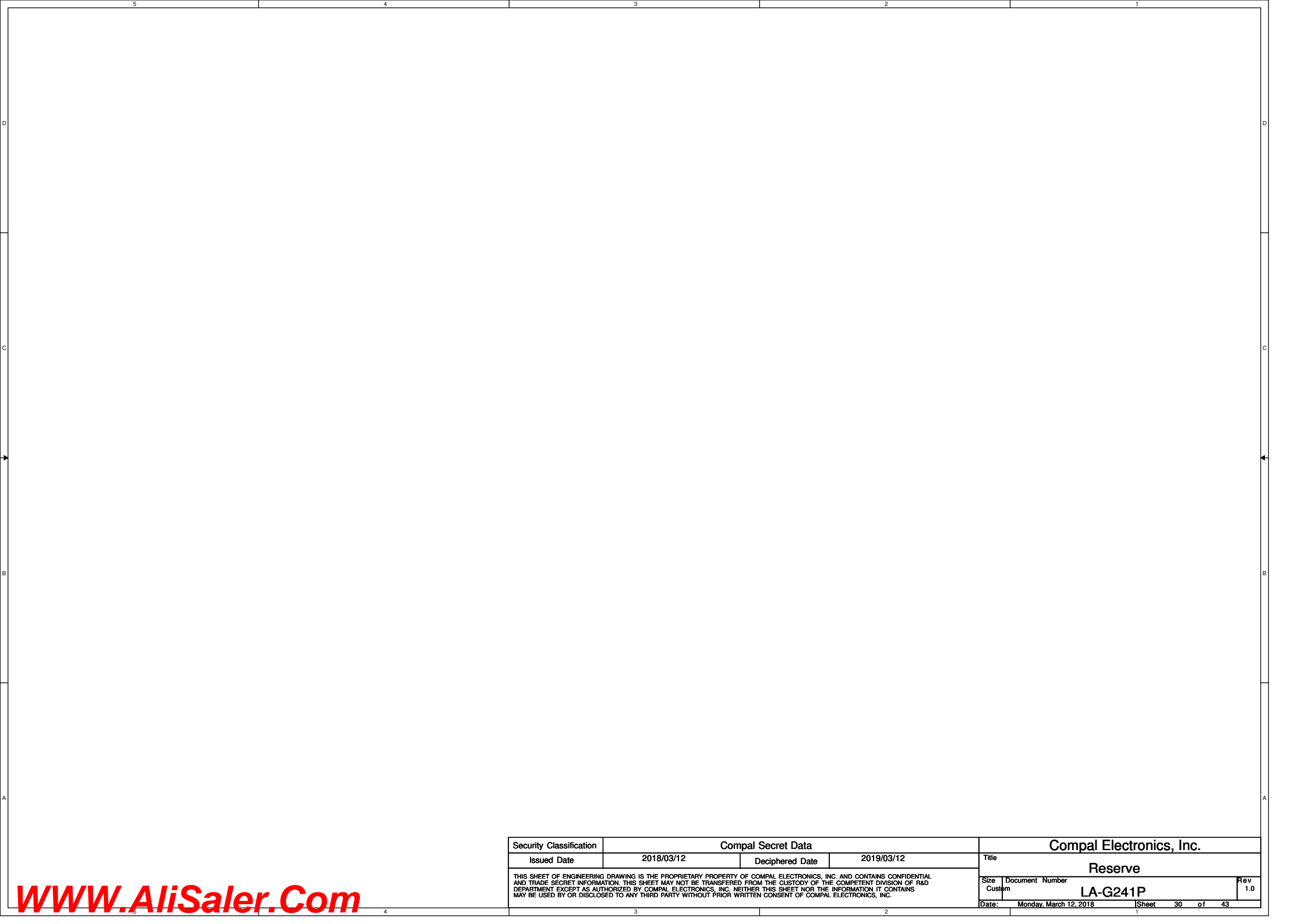
Discharge Circuit



MISC.

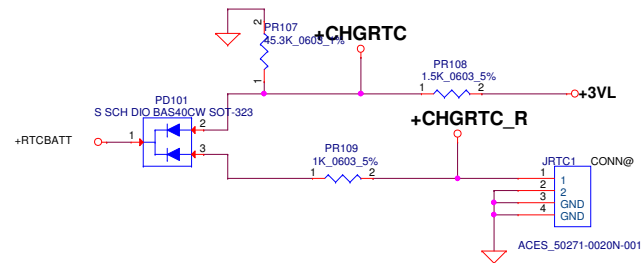
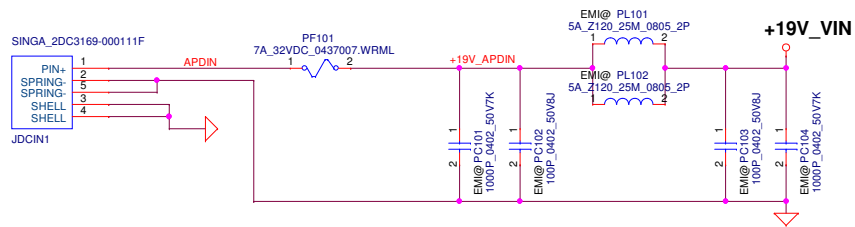


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LA-G241P				Monday, March 12, 2018	15:22:28

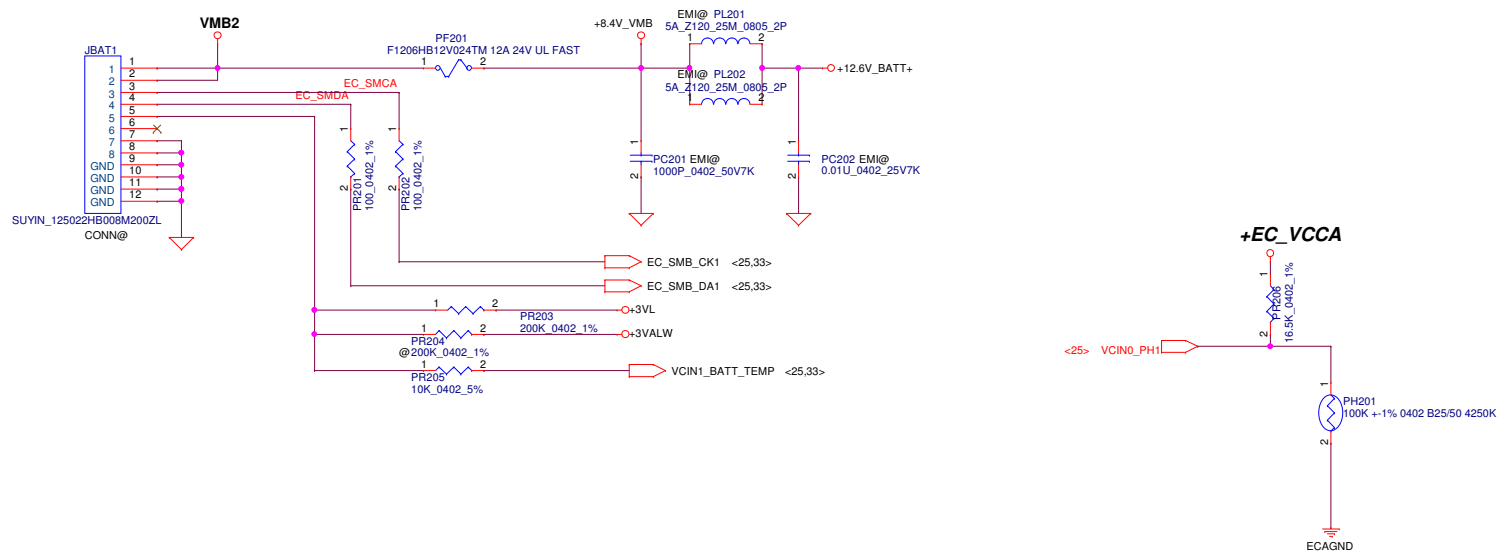


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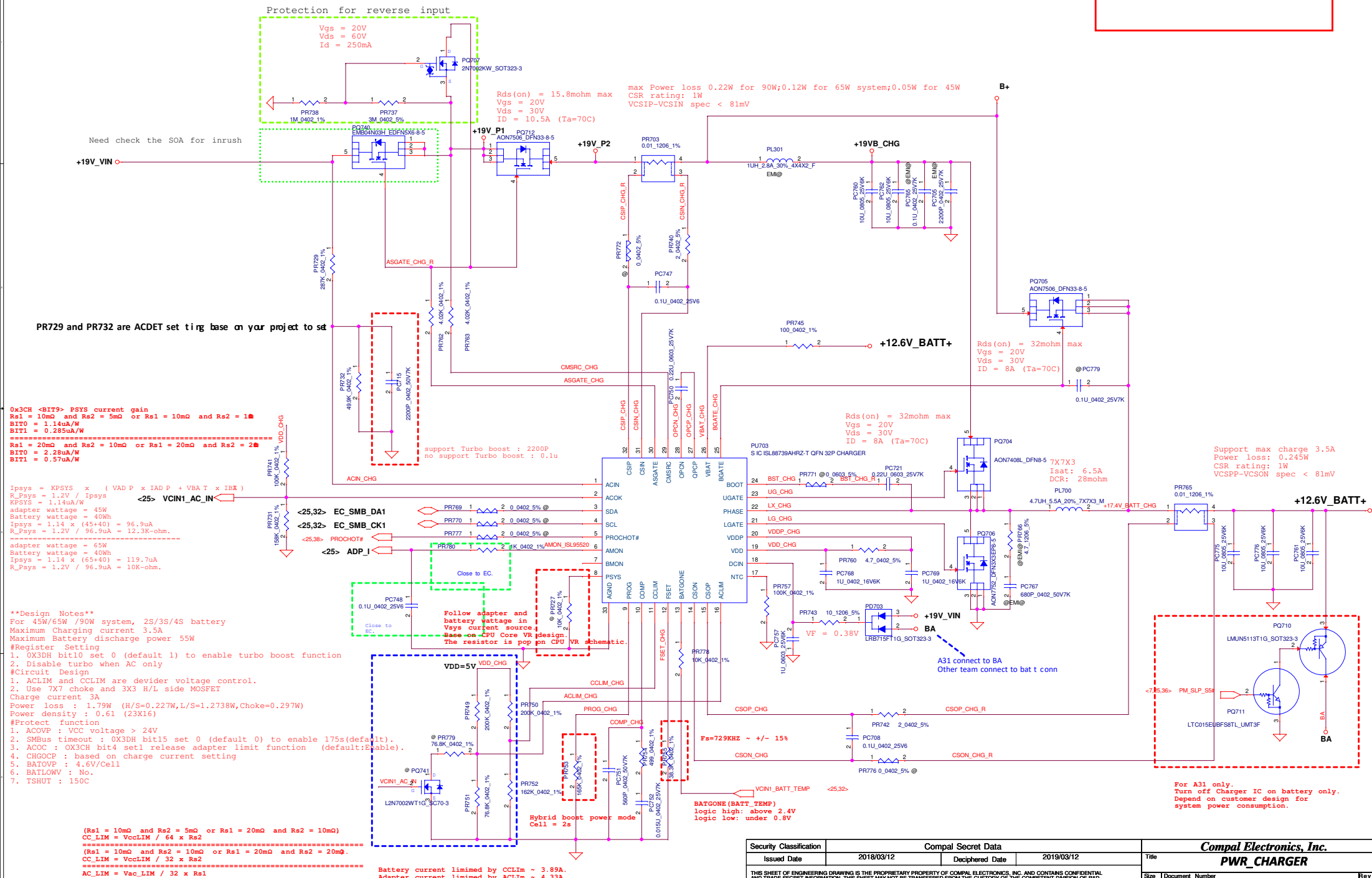


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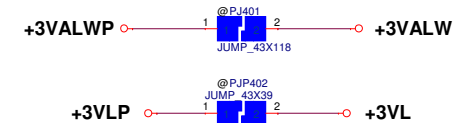


PH201 under CPU bottom side :
CPU thermal protection at 93 +/-3 degree C
Recovery at 56 +/-3 degree C

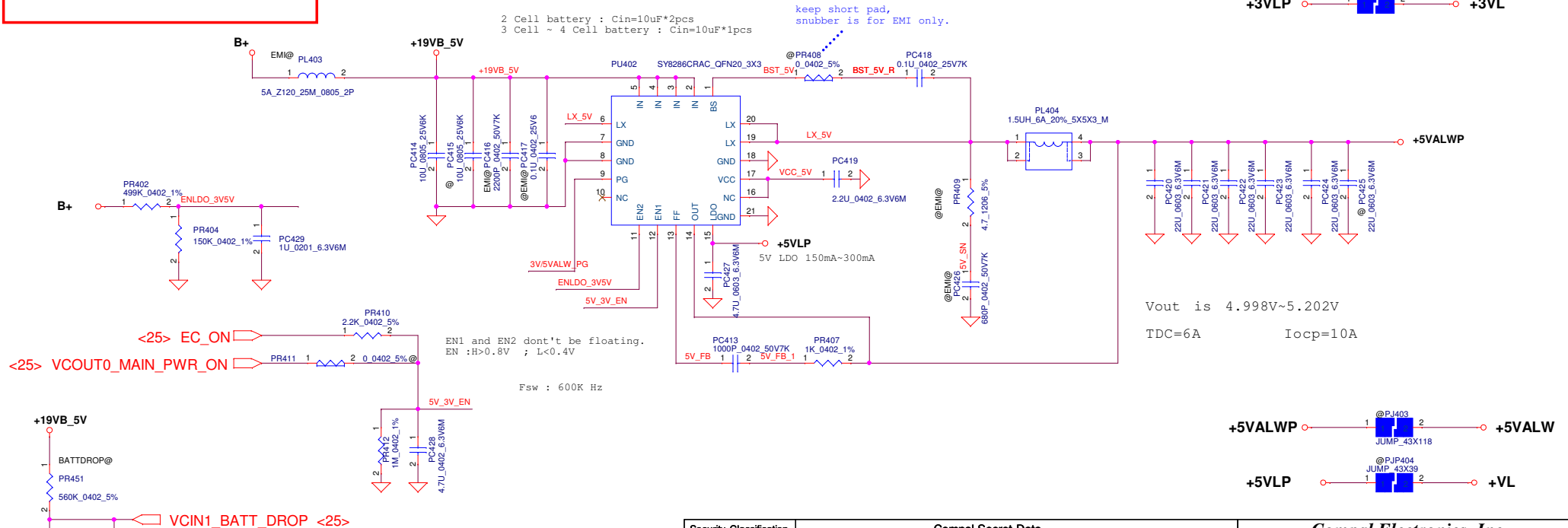
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SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd



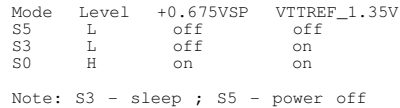
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```
RT8207P_single_V3.mdd    For Single layer
RT8207P_dual_V3.mdd     For Dual layer
```

0.675Volt	+/-	5%
TDC	0.7A	
Peak Current	1A	

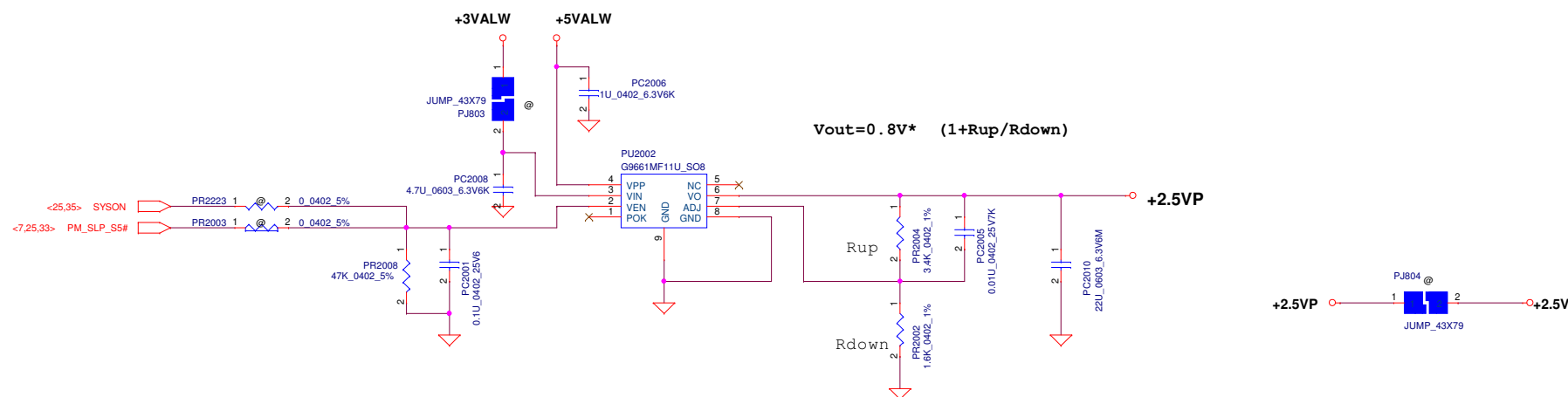
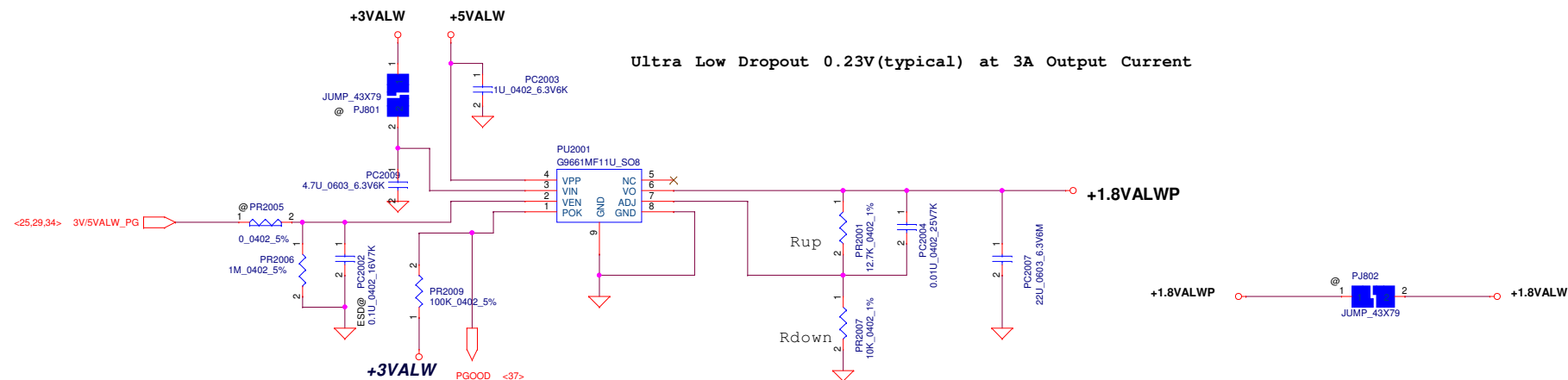


Switching Frequency: 540kHz
Ipeak=8A
Iocp~9.6A
OVP: 113%~120%
VFB=0.75V, Vout=1.3545V

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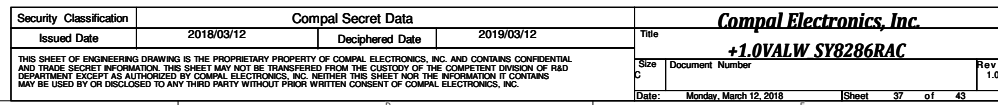
Module model information

APL5930_V2.mdd



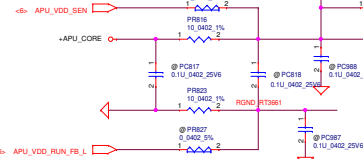
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SY8286_V2_single.mdd
SY8286_V2_dual.mdd



Module model information
RT3661AB_V2A.mdd for IC portion
RT3661AB_V2B.mdd for SW portion

PR816, PR823 are for debug only,
APU_VDD_SEN, APU_VDD_RUN_FB_L need have 10ohm at HW size.



RT3661AB SET1, TSEN and TSEN_NB Pin Setting Function:
AI VDD=100%, AI VDDNB=100%
OR Threshold: Disable
Frequency: 300kHz
VDD and VDDNB Initial Offset: 0mV (PS0)
VDD and VDDNB PHOCPP Setting Ratio: 150%

$$V_{TSEN_ADC} = 80\mu A \cdot \left[\frac{R_1 \cdot R_{NTC}}{R_1 + R_{NTC}} + \frac{R_{p1} \cdot R_{p2}}{R_{p1} + R_{p2}} \right]$$

Confirm HW side the pull high resistor

Confirm HW side the pull high resistor

LL=2.05m

25% VGATE

+3V5

10K_0402_1%

330P_0402_50V0J

PCB12

PCB13

PCB14

PCB15

PCB16

PCB17

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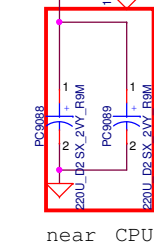
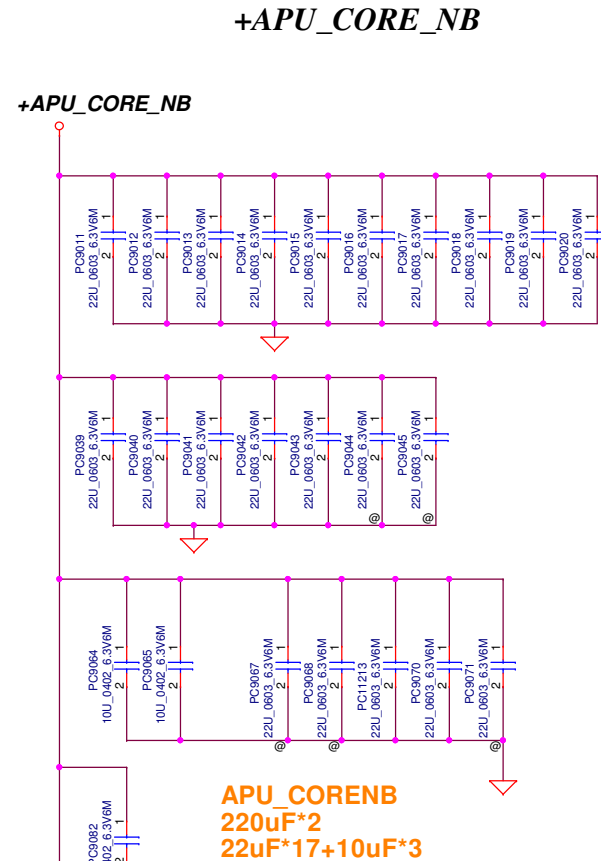
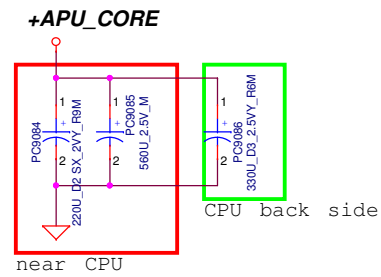
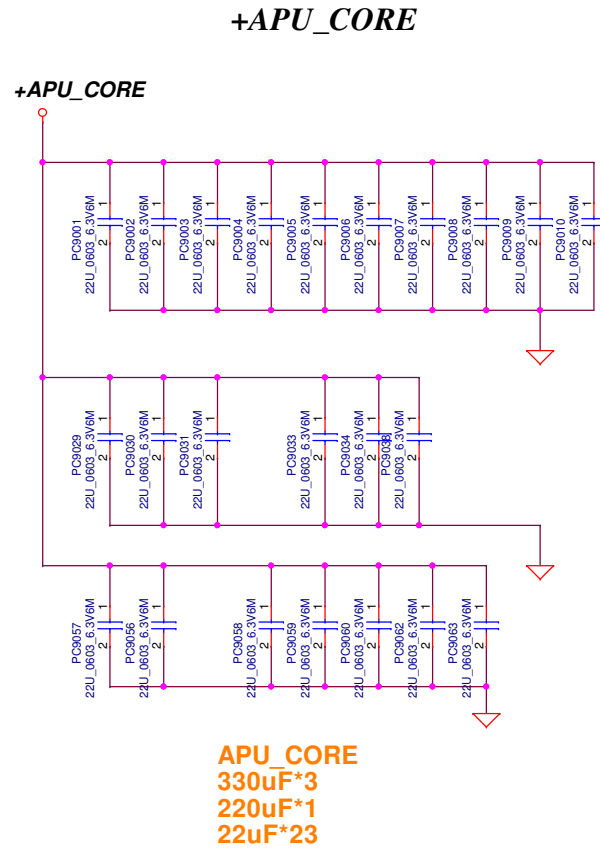
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PCB276

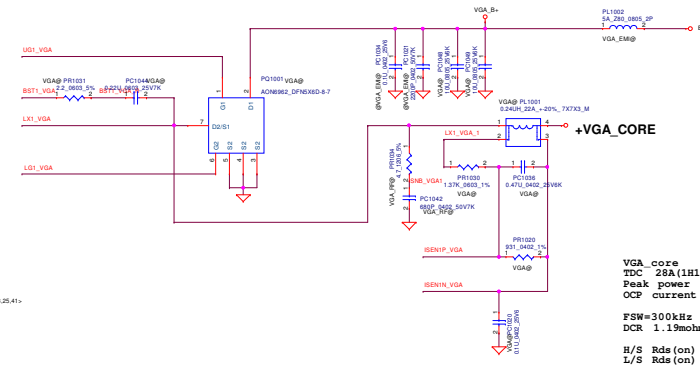
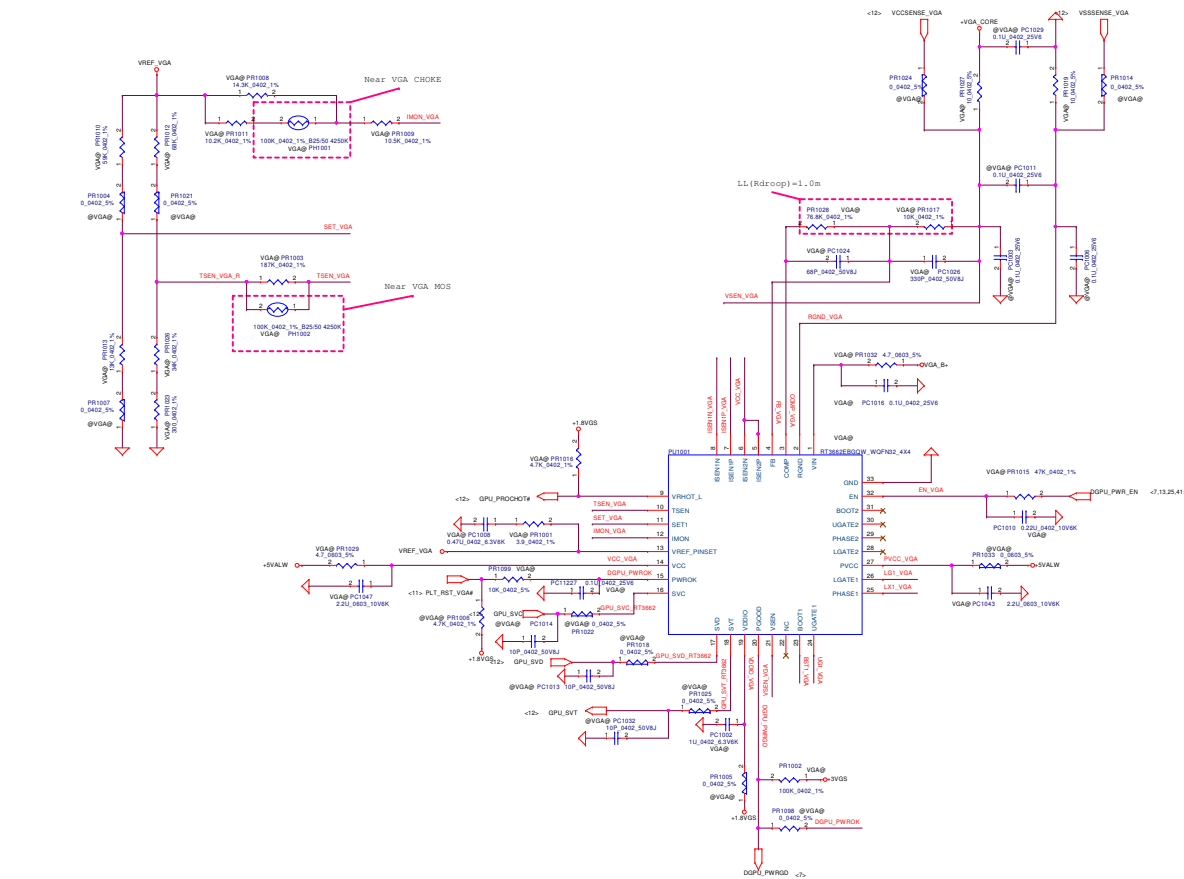
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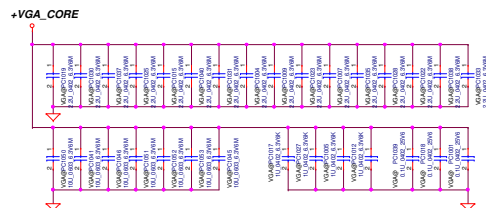
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VGA_core
 TDC 28A (1H1L)
 Peak power 38W
 OCP current > 40A
 FSW=300kHz
 DCR 1.19mohm +/-5%
 H/S Rds(on) : 6.8mohm , 8.6mohm
 L/S Rds(on) : 2.0mohm , 2.5mohm



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